Features

• DDR3 functionality and operations supported as defined in the component data sheet
• 240pin, unbuffered dual in-line memory module (UDIMM)
•Fast data transfer rates:
DDR3-1066(PC3-8500)
DDR3-1333(PC3-10600)
DDR3-1600(PC3-12800)
• Single or Dual rank
• 1GB (128 Meg x 64), 2GB (256 Meg x 64), 4GB (512Meg x 64), 8GB (1Giga x 64)
• $V_{DD} = V_{DDQ}$ = 1.5V ±0.075V
• V_{DDSPD} = 3.0V to 3.6V
• Reset pin for improved system stability
• Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
• Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
• Fly-by topology
• Terminated control, command, and address bus
• Adjustable data-output drive strength
• Serial presence-detect (SPD) EEPROM
• Gold edge contacts
• Pb-free

Module Specification (Single DIMM Package)

Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing tCL-tRCD-tRP	Operator Voltage
SP001GBLTU106S01(2)	1GB (128Mx64) 128Mx8 1Rank	PC3-8500	DDR3-1066	7-7-7	1.5V
SP001GBLTU133S01(2)		PC3-10600	DDR3-1333	9-9-9	1.5V
SP002GBLTU106S01(2)	2GB (256Mx64) 128Mx8 2Ranks	PC3-8500	DDR3-1066	7-7-7	1.5V
SP002GBLTU133S01(2)		PC3-10600	DDR3-1333	9-9-9	1.5V
SP002GBLTU160S01(2)		PC3-12800	DDR3-1600	9-9-9	1.5V
SP002GBLTU106V01(2)	2GB (256Mx64) 256Mx8 1Rank	PC3-8500	DDR3-1066	7-7-7	1.5V
SP002GBLTU133V01(2)		PC3-10600	DDR3-1333	9-9-9	1.5V
SP002GBLTU160V01(2)		PC3-12800	DDR3-1600	11-11-11	1.5V
SP004GBLTU106V01(2)	4GB (512Mx64) 256Mx8 2Ranks	PC3-8500	DDR3-1066	7-7-7	1.5V
SP004GBLTU133V01(2)		PC3-10600	DDR3-1333	9-9-9	1.5V
SP004GBLTU160V01(2)		PC3-12800	DDR3-1600	11-11-11	1.5V
SP004GBLTU133N01(2)	4GB (512Mx64) 512Mx8 1Rank	PC3-10600	DDR3-1333	9-9-9	1.5V
SP004GBLTU160N01(2)		PC3-12800	DDR3-1600	11-11-11	1.5V
SP008GBLTU133N01(2)	8GB (1Gx64) 512Mx8 2Ranks	PC3-10600	DDR3-1333	9-9-9	1.5V
SP008GBLTU160N01(2)		PC3-12800	DDR3-1600	11-11-11	1.5V
SP001GBLTU106T01(2)	1GB (128Mx64) 128Mx16 1Rank	PC3-8500	DDR3-1066	7-7-7	1.5V
SP001GBLTU133T01(2)		PC3-10600	DDR3-1333	9-9-9	1.5V
SP001GBLTU160T01(2)		PC3-12800	DDR3-1600	11-11-11	1.5V
SP002GBLTU106T01(2)	2GB (256Mx64) 128Mx16 2Ranks	PC3-8500	DDR3-1066	7-7-7	1.5V
SP002GBLTU133T01(2)		PC3-10600	DDR3-1333	9-9-9	1.5V
SP002GBLTU160T01(2)		PC3-12800	DDR3-1600	11-11-11	1.5V
SP002GBLTU106W01(2)	2GB (256Mx64) 256Mx16 1Rank	PC3-8500	DDR3-1066	7-7-7	1.5V
SP002GBLTU133W01(2)		PC3-10600	DDR3-1333	9-9-9	1.5V
SP002GBLTU160W01(2)		PC3-12800	DDR3-1600	11-11-11	1.5V
SP004GBLTU106W01(2)	4GB (512Mx64) 256Mx16 2Ranks	PC3-8500	DDR3-1066	7-7-7	1.5V
SP004GBLTU133W01(2)		PC3-10600	DDR3-1333	9-9-9	1.5V
SP004GBLTU160W01(2)		PC3-12800	DDR3-1600	11-11-11	1.5V

Note:

1. This document supports all LTU Series DDR3 240Pin UDIMM products.
2. Some item was being EOL in this list, Please contact with our sales Dep.
3. All part numbers end with a double-digit code is for customize use only.
   Example: SP001GBLTU133S02XX

Module Specification (Kit Package)

Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing (tCL-tRCD-tRP)	Operator Voltage
SP002GBLTU106S21(2)	1GB x 2 Kit Package	PC3-8500	DDR3-1066	7-7-7	1.5V
SP002GBLTU133S21(2)		PC3-10600	DDR3-1333	9-9-9	1.5V
SP002GBLTU106T21(2)	1GB x 2 Kit Package	PC3-8500	DDR3-1066	7-7-7	1.5V
SP002GBLTU133T21(2)		PC3-10600	DDR3-1333	9-9-9	1.5V
SP002GBLTU160T21(2)		PC3-12800	DDR3-1600	9-9-9	1.5V
SP004GBLTU106T21(2)	2GB x 2 Kit Package	PC3-8500	DDR3-1066	7-7-7	1.5V
SP004GBLTU133T21(2)		PC3-10600	DDR3-1333	9-9-9	1.5V
SP004GBLTU160T21(2)		PC3-12800	DDR3-1600	9-9-9	1.5V
SP004GBLTU106S21(2)	2GB x 2 Kit Package	PC3-8500	DDR3-1066	7-7-7	1.5V
SP004GBLTU133S21(2)		PC3-10600	DDR3-1333	9-9-9	1.5V
SP004GBLTU160S21(2)		PC3-12800	DDR3-1600	9-9-9	1.5V
SP004GBLTU106V21(2)	2GB x 2 Kit Package	PC3-8500	DDR3-1066	7-7-7	1.5V
SP004GBLTU133V21(2)		PC3-10600	DDR3-1333	9-9-9	1.5V
SP004GBLTU160V21(2)		PC3-12800	DDR3-1600	11-11-11	1.5V
SP004GBLTU106W21(2)	2GB x 2 Kit Package	PC3-8500	DDR3-1066	7-7-7	1.5V
SP004GBLTU133W21(2)		PC3-10600	DDR3-1333	9-9-9	1.5V
SP004GBLTU160W21(2)		PC3-12800	DDR3-1600	11-11-11	1.5V
SP008GBLTU106W21(2)	4GB x 2 Kit Package	PC3-8500	DDR3-1066	7-7-7	1.5V
SP008GBLTU133W21(2)		PC3-10600	DDR3-1333	9-9-9	1.5V
SP008GBLTU160W21(2)		PC3-12800	DDR3-1600	11-11-11	1.5V
SP008GBLTU106V21(2)	4GB x 2 Kit Package	PC3-8500	DDR3-1066	7-7-7	1.5V
SP008GBLTU133V21(2)		PC3-10600	DDR3-1333	9-9-9	1.5V
SP008GBLTU160V21(2)		PC3-12800	DDR3-1600	11-11-11	1.5V
SP016GBLTU133N21(2)	8GB x 2 Kit Package	PC3-10600	DDR3-1333	9-9-9	1.5V
SP016GBLTU160N21(2)		PC3-12800	DDR3-1600	11-11-11	1.5V
SP003GBLTU106S31(2)	1GB x 3 Kit Package	PC3-8500	DDR3-1066	7-7-7	1.5V
SP003GBLTU133S31(2)		PC3-10600	DDR3-1333	9-9-9	1.5V
SP006GBLTU106S31(2)	2GB x 3 Kit Package	PC3-8500	DDR3-1066	7-7-7	1.5V
SP006GBLTU133S31(2)		PC3-10600	DDR3-1333	9-9-9	1.5V
SP006GBLTU160S31(2)		PC3-12800	DDR3-1600	9-9-9	1.5V
SP006GBLTU106V31(2)	2GB x 3 Kit Package	PC3-8500	DDR3-1066	7-7-7	1.5V
SP006GBLTU133V31(2)		PC3-10600	DDR3-1333	9-9-9	1.5V
SP006GBLTU160V31(2)		PC3-12800	DDR3-1600	11-11-11	1.5V
SP012GBLTU106V31(2)	4GB x 3 Kit Package	PC3-8500	DDR3-1066	7-7-7	1.5V
SP012GBLTU133V31(2)		PC3-10600	DDR3-1333	9-9-9	1.5V

Note:

1. This document supports all LTU Series DDR3 240Pin UDIMM products.
2. Some item was being EOL in this list, Please contact with our sales Dep.
3. All part numbers end with a double-digit code is for customize use only.
   Example: SP001GBLTU133S02XX

Pin Assignments

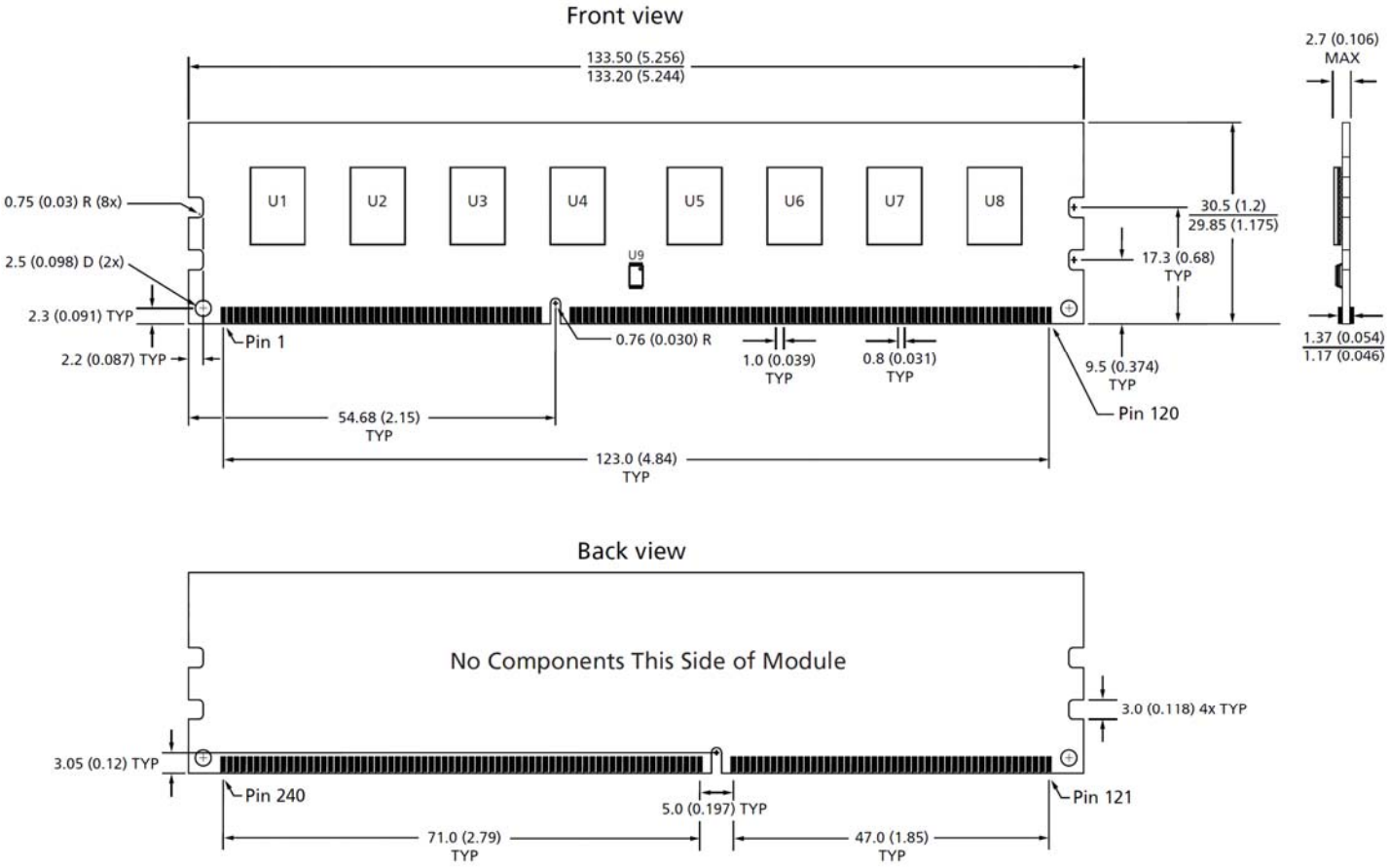
240-Pin UDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREFDQ	31	DQ25	61	A2	91	DQ41
2	VSS	32	VSS	62	VDD	92	VSS
3	DQ0	33	DQS3#	63	CK1	93	DQS5#
4	DQ1	34	DQS3	64	CK1#	94	DQS5
5	VSS	35	VSS	65	VDD	95	VSS
6	DQS0#	36	DQ26	66	VDD	96	DQ42
7	DQS0	37	DQ27	67	VREFCA	97	DQ43
8	VSS	38	VSS	68	NC	98	VSS
9	DQ2	39	NC	69	VDD	99	DQ48
10	DQ3	40	NC	70	A10	100	DQ49
11	VSS	41	VSS	71	BA0	101	VSS
12	DQ8	42	NC	72	VDD	102	DQS6#
13	DQ9	43	NC	73	WE#	103	DQS6
14	VSS	44	VSS	74	CAS#	104	Vss
15	DQS1#	45	NC	75	VDD	105	DQ50
16	DQS1	46	NC	76	S1#	106	DQ51
17	VSS	47	VSS	77	ODT1	107	VSS
18	DQ10	48	NC	78	VDD	108	DQ56
19	DQ11	49	NC	79	NC	109	DQ57
20	VSS	50	CKE0	80	VSS	110	VSS
21	DQ16	51	VDD	81	DQ32	111	DQS7#
22	DQ17	52	BA2	82	DQ33	112	DQS7
23	VSS	53	NC	83	VSS	113	VSS
24	DQS2#	54	VDD	84	DQS4#	114	DQ58
25	DQS2	55	A11	85	DQS4	115	DQ59
26	VSS	56	A7	86	VSS	116	VSS
27	DQ18	57	VDD	87	DQ34	117	SA0
28	DQ19	58	A5	88	DQ35	118	SCL
29	VSS	59	A4	89	VSS	119	SA2
30	DQ24	60	VDD	90	DQ40	120	VTT

240-Pin UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
121	VSS	151	VSS	181	A1	211	VSS
122	DQ4	152	DM3	182	VDD	212	DM5
123	DQ5	153	NC	183	VDD	213	NC
124	VSS	154	VSS	184	CK0	214	VSS
125	DM0	155	DQ30	185	CK0#	215	DQ46
126	NC	156	DQ31	186	VDD	216	DQ47
127	VSS	157	VSS	187	NC	217	VSS
128	DQ6	158	NC	188	A0	218	DQ52
129	DQ7	159	NC	189	VDD	219	DQ53
130	VSS	160	VSS	190	BA1	220	VSS
131	DQ12	161	NC	191	VDD	221	DM6
132	DQ13	162	NC	192	RAS#	222	NC
133	VSS	163	VSS	193	S0#	223	VSS
134	DM1	164	NC	194	VDD	224	DQ54
135	NC	165	NC	195	ODT0	225	DQ55
136	VSS	166	VSS	196	A13	226	VSS
137	DQ14	167	NC	197	VDD	227	DQ60
138	DQ15	168	RESET#	198	NC	228	DQ61
139	VSS	169	CKE1	199	VSS	229	VSS
140	DQ20	170	VDD	200	DQ36	230	DM7
141	DQ21	171	NC	201	DQ37	231	NC
142	VSS	172	NC/A14	202	VSS	232	VSS
143	DM2	173	VDD	203	DM4	233	DQ62
144	NC	174	A12	204	NC	234	DQ63
145	VSS	175	A9	205	VSS	235	VSS
146	DQ22	176	VDD	206	DQ38	236	VDDSPD
147	DQ23	177	A8	207	DQ39	237	SA1
148	VSS	178	A6	208	VSS	238	SDA
149	DQ28	179	VDD	209	DQ44	239	VSS
150	DQ29	180	A3	210	DQ45	240	VTT

Pin Description

Symbol	Type	Description
A0–A14	Input	**Address inputs:** Provide the row address for ACTIVE commands and the column address and auto precharge bit for READ/WRITE commands to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. The address inputs also provide the opcode during mode register command set. A0–A13 (128Mx8, 128Mx16) A0–A14 (256Mx8, 256Mx16) A0–A15 (512Mx8).
BA0–BA2	Input	**Bank address inputs:** BA0, BA1 define to which device bank an ACTIVE, READ, WRITE, orPRECHARGE command is being applied. BA0, BA1 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command.
CK0, CK0#, CK1, CK1#	Input	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE0, CKE1	Input	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR3 SDRAM.
DM0–DM7	Input	**Data input mask:** DM is an input mask signal for write data. Input data is masked when DM issampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS7pins.
ODT0 ODT1	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to the following pins: DQ, DQS, DQS# and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 ×V_{DD} and DC LOW ≤ 0.2 ×V_{DD}.
S0#, S1#	Input	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[2:0]	Input	**Presence-detect address inputs:** These pins are used to configure the SPD EEPROM address range.
SCL	Input	**Serial clock for presence-detect:** SCL is used to synchronize the presence-detect data transfer to and from the module.
DQ0–DQ63	I/O	**Data input/output:** Bidirectional data bus.
DQS0–DQS7 DQS0#–DQS7#	I/O	**Data strobe:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data.
SDA	I/O	**Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the SPD EEPROM on the module.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V. The component V_{DD} and V_{DDQ} are connected to the module V_{DD}.
V_{DDSPD}	Supply	**Temperature sensor/SPD EEPROM power supply:** +3.0V to +3.6V.
V_{REFCA}	Supply	**Reference voltage:** Control, command, and address (V_{DD}/2).
V_{REFDQ}	Supply	**Reference voltage:** DQ, DM (V_{DD}/2).
V_{SS}	Supply	Ground.
V_{TT}	Supply	**Termination voltage:** Used for control, command, and address (V_{DD}/2).
NC	–	**No connect:** These pins are not connected on the module.
NU	–	**Not used:** These pins are not used in specific module configuration/operations.

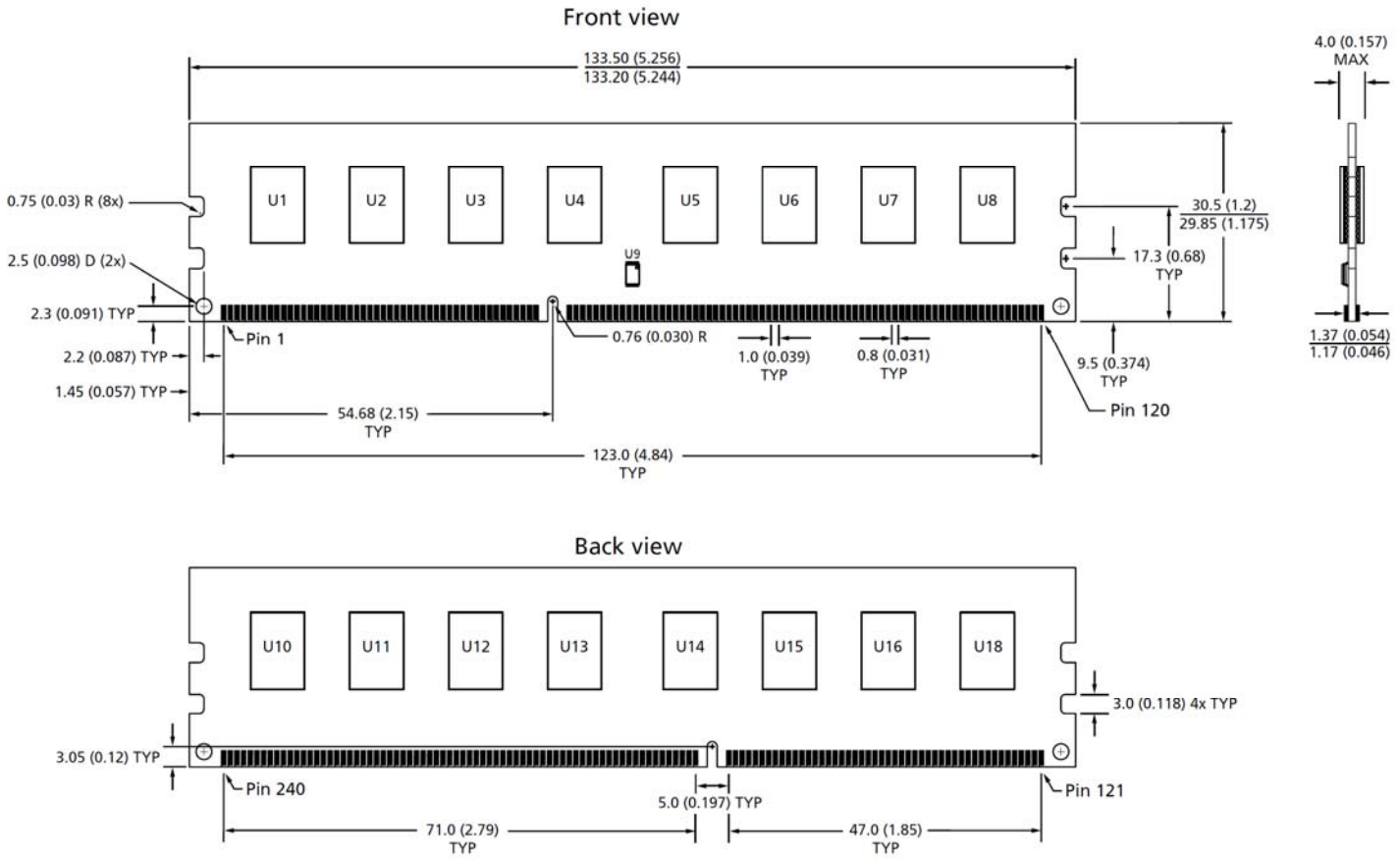
Simplified Mechanical Drawing(x8 1Rank)



Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.

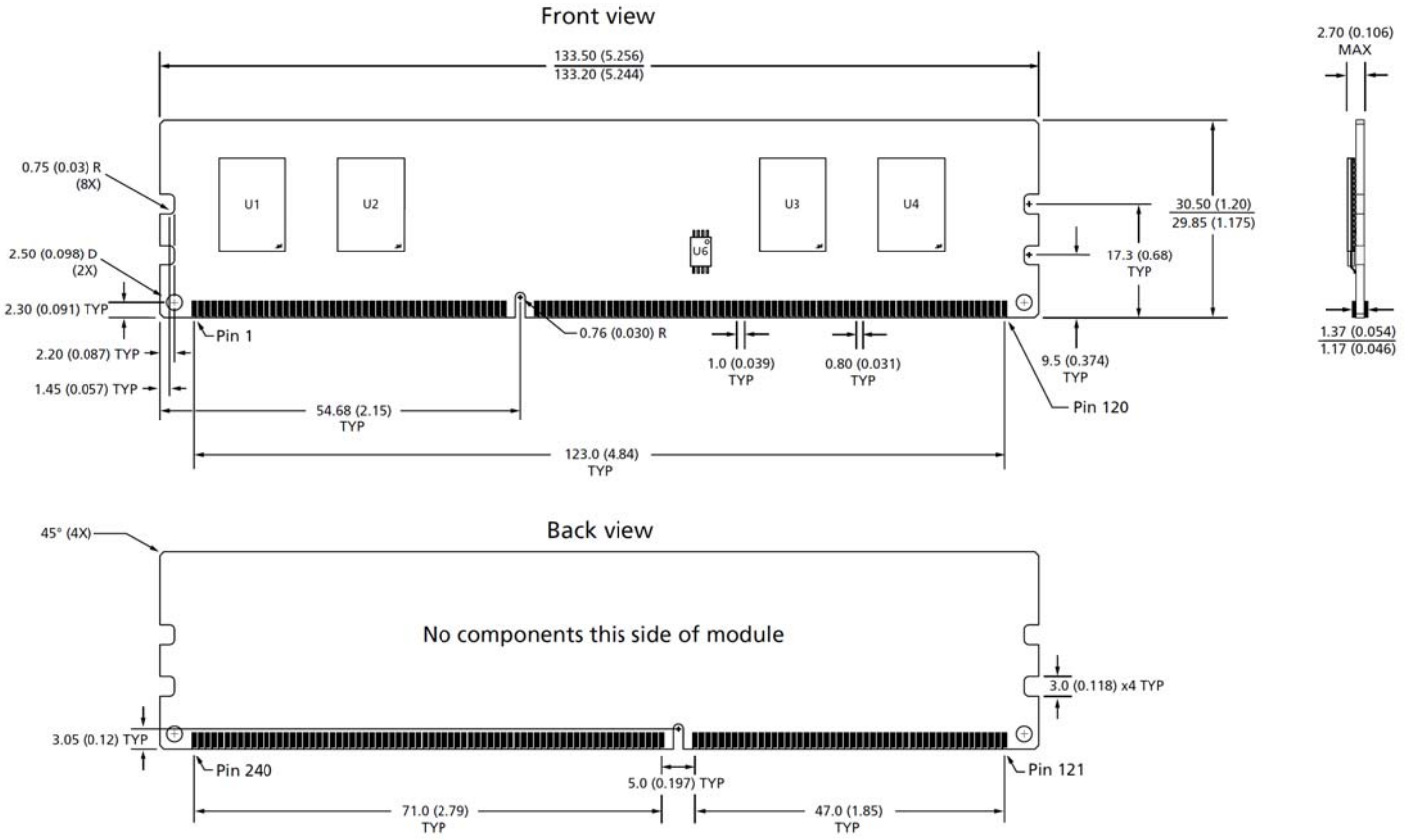
Simplified Mechanical Drawing(x8 2Ranks)



Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.

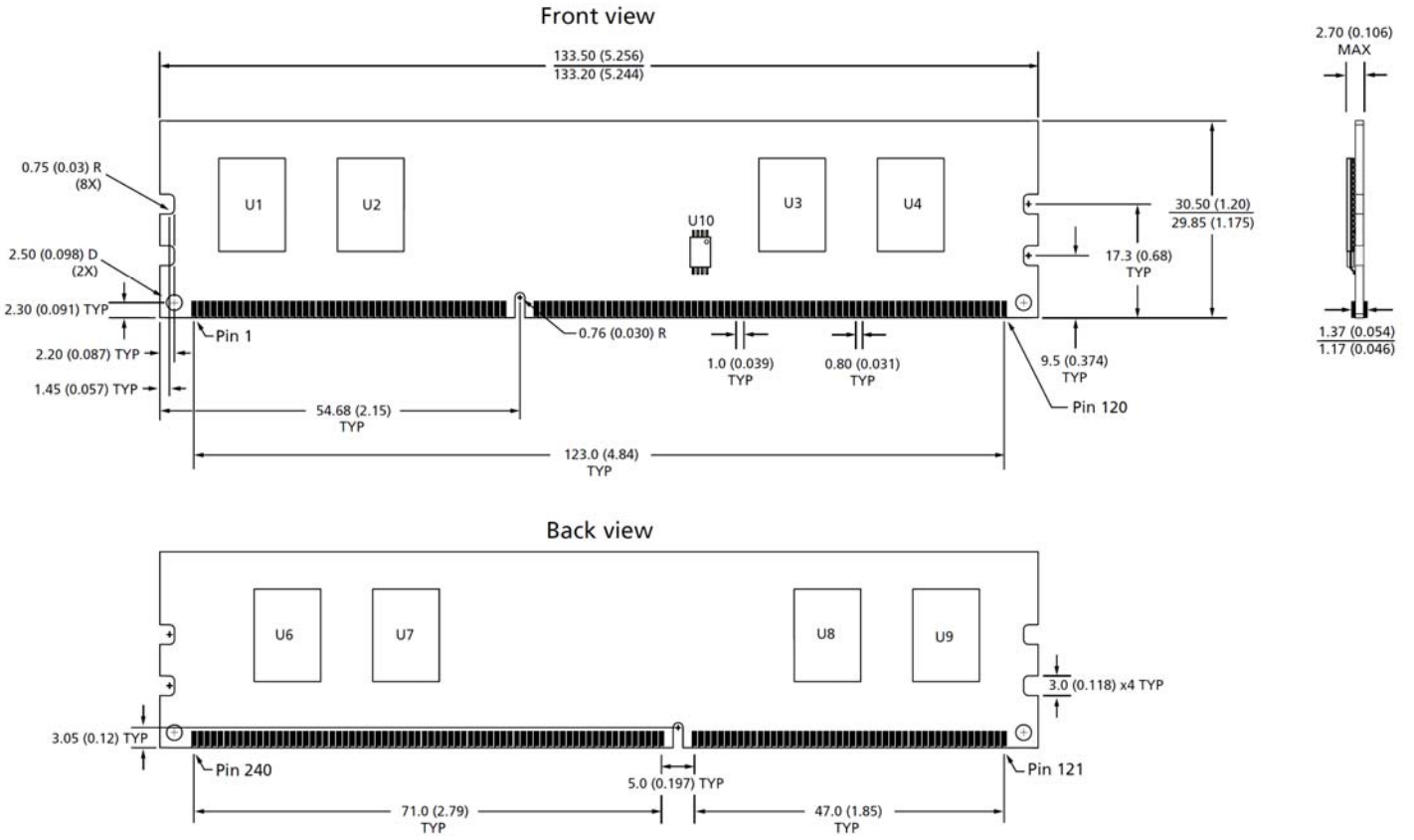
Simplified Mechanical Drawing(x16 1Rank)



Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.

Simplified Mechanical Drawing(x16 2Ranks)



Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.