



Data Sheet

VT6421A *Serial ATA RAID Controller*

(Released under Creative Commons License)
Preliminary Revision 1.0
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VIA TECHNOLOGIES, INC.

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Offices:

VIA Technologies Incorporated
Taiwan Office:
1st Floor, No. 531
Chung-Cheng Road, Hsin-Tien
Taipei, Taiwan ROC
Tel: 886-2-2218-5452
FAX: 886-2-2218-5453
Home page: <http://www.via.com.tw>

VIA Technologies Incorporated
USA Office:
940 Mission Court
Fremont, CA 94539
USA
Tel: 510-683-3300
FAX: 510-683-3301 or 510-687-4654
Home Page: <http://www.viatech.com>

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VT6421A

Serial ATA RAID Controller

PRODUCT FEATURES

- **RAID Controller**
 - Supports RAID Level 0, RAID Level 1, RAID 0+1 and JBOD
- **Serial ATA Interface**
 - Complies with Serial ATA Specification Revision 1.0
 - Supports internal PHY, with each PHY supporting up to two S-ATA devices
 - Dual channel master mode supporting up to two S-ATA devices. The S-ATA drive transfer rate is capable up to 150 MB/s per channel
- **PCI interface**
 - 33 MHz operation
 - Supports PCI 2X mode
 - Supports PCI native modes
 - Complies with PCI Local Bus Specification Revision 2.2
- **UltraATA-133 / IDE interface**
 - Single channel master mode hard disk controller supporting two enhanced IDE devices
 - Redefined Bus Master Programming Interface for IDE controllers to support up to four bus masters in a single function
 - Supports ATA PIO mode 4, multi-word DMA-mode 2 drivers and UltraDMA-mode6
 - Extension to UltraDMA-133 interface for up to 133MB/sec transfer rate
 - Complies with ATA/ATAPI-6
- **BIOS expansion**
 - Supports external FLASH or EEPROM for BIOS expansion and RAID functions
- **Clock Input**
 - 33MHz for PCI operation
 - External Crystal input for S-ATA port operation
- **Power Supply**
 - 3.3V for PCI and IDE operation
 - 2.5V for Oscillator and Serial ATA port operation
- **0.22 μ m, lower power CMOS process**
- **14x20 mm, 128-pin LQFP**

OVERVIEW

The VT6421A is a high performance S-ATA RAID Controller that supports RAID Level 0, RAID Level 1, RAID 0+1 and JBOD. The VT6421A complies with Serial ATA Specification Revision 1.0 and includes two internal Serial ATA PHY interfaces, with each PHY supporting up to two S-ATA devices. The device uses a PCI interface that complies with PCI Specification Revision 2.2. This device also redefined Bus Master Programming Interface for the IDE controllers to support up to four bus masters in a single function.

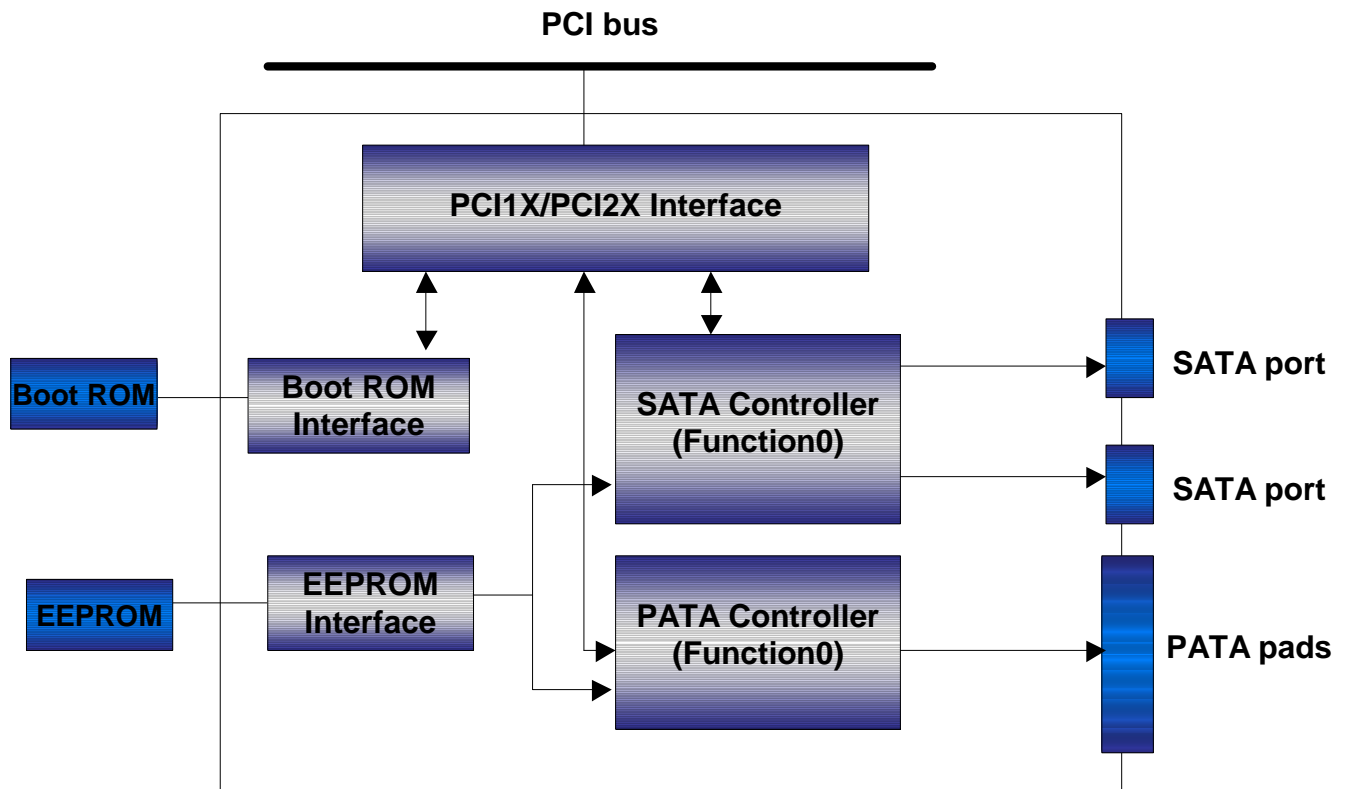


Figure 1. VT6421A Block Diagram

PINOUTS

Pin Diagram

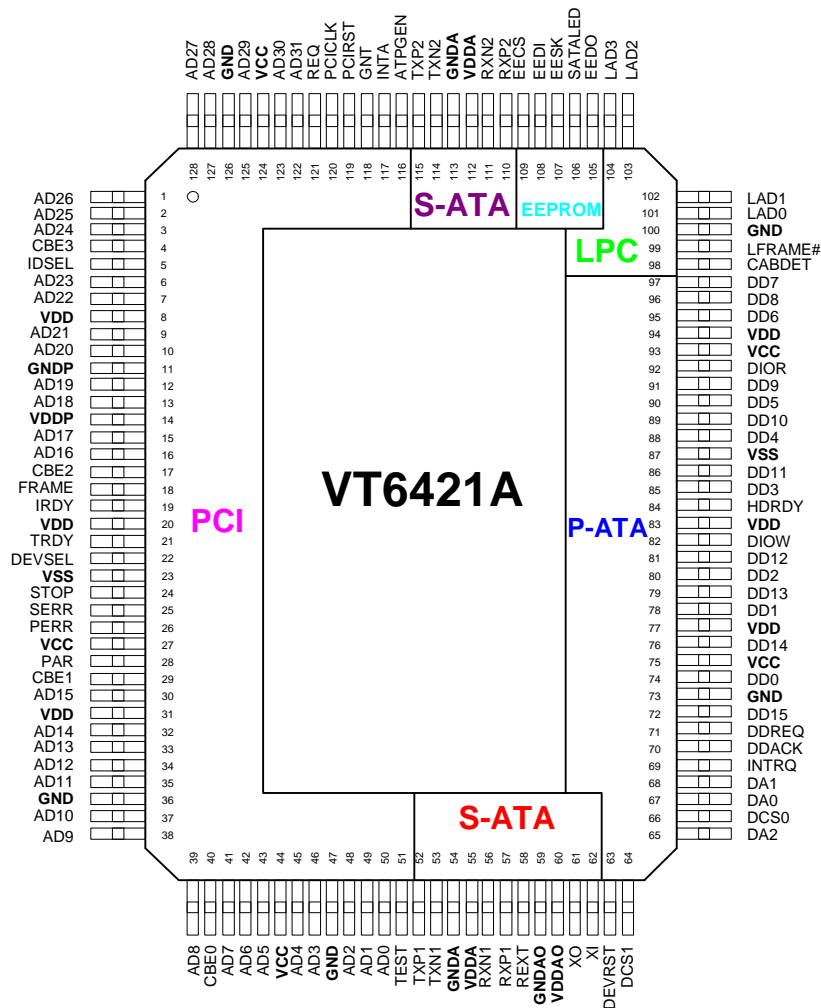


Figure 2. VT6421A Pin Diagram (Top View)

Pin List
Table 1. Pin List (Listed by Pin Name)

Pin Name	Pin#	Type	Pin Name	Pin#	Type	Pin Name	Pin#	Type	Pin Name	Pin#	Type
AD00	50	DIO	ATPGEN	116	DI	DIOW	82	DO	RXN1	56	DI
AD01	49	DIO	CABDET	98	DI	EECS	109	DO	RXN2	111	DI
AD02	48	DIO	CBE0	40	DIO	EEDI	108	DO	RXP1	57	DI
AD03	46	DIO	CBE1	29	DIO	EEDO	105	DI	RXP2	110	DI
AD04	45	DIO	CBE2	17	DIO	EESK	107	DO	SATALED	106	DO
AD05	43	DIO	CBE3	4	DIO	FRAME	18	DIO	SERR	25	DI
AD06	42	DIO	DA0	67	DIO	GND	36	P	STOP	24	DIO
AD07	41	DIO	DA1	68	DIO	GND	47	P	TEST	51	DI
AD08	39	DIO	DA2	65	DIO	GND	73	P	TRDY	21	DIO
AD09	38	DIO	DCS0	66	DO	GND	100	P	TXN1	53	DO
AD10	37	DIO	DCS1	64	DO	GND	126	P	TXN2	114	DO
AD11	35	DIO	DD00	74	DIO	GNDA	54	P	TXP1	52	DO
AD12	34	DIO	DD01	78	DIO	GNDA	113	P	TXP2	115	DO
AD13	33	DIO	DD02	80	DIO	GNDAO	59	P	VCC	27	P
AD14	32	DIO	DD03	85	DIO	GNDP	11	P	VCC	44	P
AD15	30	DIO	DD04	88	DIO	GNT	118	DIO	VCC	75	P
AD16	16	DIO	DD05	90	DIO	HDRDY	84	DI	VCC	93	P
AD17	15	DIO	DD06	95	DIO	IDSEL	5	DIO	VCC	124	P
AD18	13	DIO	DD07	97	DIO	INTA	117	DO	VDD	8	P
AD19	12	DIO	DD08	96	DIO	INTRQ	69	DI	VDD	20	P
AD20	10	DIO	DD09	91	DIO	IRDY	19	DIO	VDD	31	P
AD21	9	DIO	DD10	89	DIO	LAD0	101	DIO	VDD	77	P
AD22	7	DIO	DD11	86	DIO	LAD1	102	DIO	VDD	83	P
AD23	6	DIO	DD12	81	DIO	LAD2	103	DIO	VDD	94	P
AD24	3	DIO	DD13	79	DIO	LAD3	104	DIO	VDDA	55	P
AD25	2	DIO	DD14	76	DIO	LFRAME#	99	DO	VDDA	112	P
AD26	1	DIO	DD15	72	DIO	PAR	28	DIO	VDDAO	60	P
AD27	128	DIO	DDACK	70	DO	PCICLK	120	DIO	VDDP	14	P
AD28	127	DIO	DDREQ	71	DI	PCIRST	119	DIO	VSS	23	P
AD29	125	DIO	DEVIRST	63	DO	PERR	26	DI	VSS	87	P
AD30	123	DIO	DEVSEL	22	DIO	REQ	121	DIO	XI	62	DI
AD31	122	DIO	DIOR	92	DO	REXT	58	DI	XO	61	DO

Note: D = Digital, A = Analog, I = Input, O = Output, P = Power / Ground

Pin Descriptions
Table 2. Pin Descriptions

PCI Interface				
Signal Name	Pin #	I/O	Power	Signal Description
AD[31:0]	See Pin List	DIO	VCC	Address and Data. Multiplexed address and data. The address is driven with FRAME assertion and the data is driven or received in subsequent cycles.
CBE[3:0]	4, 17, 29, 40	DIO	VCC	Command / Byte Enable. The command for the current cycle is driven with FRAME assertion. Byte enables corresponding to supply or request data are then driven on following clocks.
PAR	28	DIO	VCC	Parity. A single parity bit is provided for the AD[31:0] and CBE[3:0] to check if the data has been transferred accurately.
IDSEL	5	DIO	VCC	Initialization Device Select. Used as a chip select during configuration read and write cycles.
DEVSEL	22	DIO	VCC	Device Select. As an output, this signal is asserted to claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL indicates the response to a VT6421A-initiated transaction and is also sampled when decoding whether to subtractive decode the cycle.
FRAME	18	DIO	VCC	Cycle Frame. Assertion indicates the address phase of a PCI transfer. Negation indicates that the cycle initiator desires one more data transfer.
STOP	24	DIO	VCC	PCI Stop. Asserted by the target to request the master (PCI device) to stop the current transaction.
IRDY	19	DIO	VCC	Initiator Ready. Asserted when the initiator is ready for data transfer.
TRDY	21	DIO	VCC	Target Ready. Asserted when the target is ready for data transfer.
SERR	25	DIO	VCC	System Error. SERR can be pulsed active by any PCI device that detects a system error condition.
PERR	26	DIO	VCC	Parity Error. Asserted when data parity error occurs during all PCI transitions except a special cycle.
REQ	121	DIO	VCC	PCI Bus Request. Asserted by the VT6421A to request bus use.
GNT	118	DIO	VCC	PCI Bus Grant. Asserted by the bus arbiter to grant permission to the VT6421A for access to the PCI bus for bus master operations.
PCIRST	119	DIO	VCC	PCI Reset. When detected low, an internal hardware reset is performed. PCIRST# assertion or de-assertion may be asynchronous to PCICLK, however, it is recommended that de-assertion be synchronous to guarantee a clean and bounce free edge.
PCICLK	120	DIO	VCC	PCI Clock. 33 MHz. Used to clock all PCI bus transactions.
INTA	117	DO	VCC	PCI Interrupts. Asynchronous signal used to request an interrupt.

Note: DI = Digital Input, DO = Digital Output, DIO = Digital I/O, OD = Digital "Open Drain" Output, P = Power / Ground

Serial ATA Interface				
Signal Name	Pin #	I/O	Power	Signal Description
RXN1	56	DI	VDDA	S-ATA Primary Channel Differential Receive-.
RXN2	111	DI	VDDA	S-ATA Secondary Channel Differential Receive-.
RXP1	57	DI	VDDA	S-ATA Primary Channel Differential Receive+.
RXP2	110	DI	VDDA	S-ATA Secondary Channel Differential Receive+.
TXN1	53	DO	VDDA	S-ATA Primary Channel Differential Transmit-.
TXN2	114	DO	VDDA	S-ATA Secondary Channel Differential Transmit-.
TXP1	52	DO	VDDA	S-ATA Primary Channel Differential Transmit+.
TXP2	115	DO	VDDA	S-ATA Secondary Channel Differential Transmit+.
XI	62	DI	VDDAO	Crystal XI.
XO	61	DO	VDDAO	Crystal XO.
REXT	58	DI	-	External Resistor for Bandgap.
SATALED	106	DO	VCC	SATA LED.

Parallel-ATA Interface				
Signal Name	Pin #	I/O	Power	Signal Description
HDRDY	84	DI	VCC	EIDE Mode: Primary I/O Channel Ready. Device ready indicator
				UltraDMA Mode: Device DMA Ready. Channel output flow control. The device may assert DDMARDY to pause output transfers Device Strobe. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
DIOR	92	DO	VCC	EIDE Mode: Primary Device I/O Read. Device read strobe
				UltraDMA Mode: Host DMA Ready. Channel input flow control. The host may assert HDMARDY to pause input transfers. Host Strobe. Output data strobe (both edges). The host may stop HSTROBE to pause output data transfers
DIOW	82	DO	VCC	EIDE Mode: Primary Device I/O Write. Device write strobe
				UltraDMA Mode: Device Stop. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
DDREQ	71	DI	VCC	Primary Device DMA Request.
DDACK	70	DO	VCC	Primary Device DMA Acknowledge.
INTRQ	69	DI	VCC	Primary Device Interrupt.
DCS0	66	DO	VCC	Primary Device Chip Select 1. Select the command block register.
DCS1	64	DO	VCC	Primary Device Chip Select 3. Select the control block register.
DA[2:0]	65, 67, 68	DO	VCC	Primary Device Address. PDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
DD[15:0]	See Pin List	DIO	VCC	Primary Device Data.
DEVRST	63	DO	VCC	Primary Device Reset.
CABDET	98	DI	VCC	Primary Cable Detect.

LPC ROM Interface				
Signal Name	Pin #	I/O	Power	Signal Description
LFRAME#	99	DO	VCC	LPC Frame. This signal indicates the start of an LPC cycle.
LAD[3:0]	101, 102, 103, 104	DIO	VCC	LPC Address / Data 3 – 0. 4-bit LPC address / bi-directional data lines. LAD0 is the lsb and LAD3 is the msb.

EEPROM Interface				
Signal Name	Pin #	I/O	Power	Signal Description
EECS	109	DO	VCC	EEPROM Chip Select.
EEDI	108	DO	VCC	EEPROM Data In.
EESK	107	DO	VCC	EEPROM Clock.
EEDO	105	DI	VCC	EEPROM Data Out.

Power and Ground			
Signal Name	Pin #	I/O	Signal Description
VCC	27,44,75,93,124	P	PCI I/O 3.3V power.
VDD	8, 20, 31,77, 83,94	P	Core 2.5V Power.
GND	36,47,73,100,126	P	PCI I/O Ground.
VSS	23,87	P	Core Ground.
VDDP	14	P	PCI APLL Analog 2.5V power.
GNDP	11	P	PCI APLL Analog ground.
VDDA	55, 112	P	S-ATA TX/RX 2.5 power.
GND A	54, 113	P	S-ATA TX/RX ground.
VDDAO	60	P	S-ATA APLL Analog 2.5V power.
GND AO	59	P	S-ATA APLL Analog ground

REGISTERS

Register Overview

The following tables summarize all on-chip registers. These tables also document the power-on default value (“Default”) and access type (“Acc”) for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), “—” for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1’s to Clear individual bits). Registers indicated as RW may have some read/only bits that always reads back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details).

Detailed register descriptions are provided in the following section of this document. All offset and default values are shown in hexadecimal unless otherwise indicated.

Table 3. Register Summary

Serial ATA Function 0 Registers

Configuration Header Registers

Offset	Serial ATA Function 0	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	3249	RO
5-4	PCI Command	0000	RW
7-6	PCI Status	0290	RW
8	Revision ID	80	RO
9	Programming Interface	8F	RO
A	Sub Class	04	RO
B	Base Class	01	RO
C	Cache Line Size	00	RO
D	Latency Timer	20	RW
E	Header Type	00	RO
F	Fixed at 0	00	RO
13-10	S-ATA Primary Data / Command, Control / Status Base Address	AF0	RW
17-14	S-ATA Secondary Data / Command, Control / Status Base Address	A70	RW
1B-18	PATA Data / Command, Control / Status Base Address	1F0	RW
1F-1C	Reserved Data / Command, Control / Status Base Address	170	RW
23-20	Bus Master Mode Base Address	CC00	RW
27-24	S-ATA Ctrl / Status Base Address	8C00	RW
2F-2C	Sub System ID	32491106	RO
33-30	Expansion ROM Base	0000	RW
34	PCI Power Mgmt Capability Pointer	E0	RO
3C	Interrupt Line	00	RW
3D	Interrupt Pin	01	RO
40	S-ATA Channel Enable	03	RW
41	S-ATA Interrupt Gating	03	RW
42	Native Mode Enable	F1	RW
43	FIFO Threshold Control	40	RW
44	Miscellaneous Control I	06	RW
45	Miscellaneous Control II	9F	RW
46	Miscellaneous Control III	00	RW
47	-reserved-	00	RO
48	Internal PHY Wake-up	00	RW
49	Strapping Status	00	RW
4A	-reserved-	00	RO
4B	-reserved-	00	RO
4E	Internal PHY Error Status	00	RW
4F	Error Status Output Enable Control	00	RW

Transport Registers

Offset	Transport Control	Default	Acc
50	Software Ctrl Power Mode Request	00	RW
51	Hardware Ctrl Power Mode	00	RW
52	Transport Miscellaneous Control	00	RW
53	Slave Mode Testing	00	RW

Link Registers

Offset	Link Control	Default	Acc
54	-reserved-	00	RO
55	Internal PHY Look Back Test	00	RW
56	Internal PHY S-ATA LINK Control	00	RW
57	-reserved-	00	RO

PHY Registers

Offset	PHY Control	Default	Acc
58	Internal PHY Test Mode Control	00	RW
59	Test Pattern Repeat Number	10	RW
5A	Internal PHY Control	10	RW
5B	-reserved-	00	RO
5C	Internal PHY Control	05	RW
5D	PHY Direct Access Mode Control	00	RW
5E	S-ATA Internal PHY Pad Control	00	RW

RAMBIST Registers

Offset	RAMBIST Control	Default	Acc
5F	RAMBIST	00	RW

BROM Registers

Offset	BROM Control	Default	Acc
63-60	Boot ROM Address	00000000	RW
67-64	Boot ROM Read / Write Data	00000000	RW
68	BROM Access Control	00	RW
69	BROM Error Status	00	RO

EEPROM Registers

Offset	EEPROM Control	Default	Acc
6C	EEPROM Access Control	00	RW
6F-6E	EEPROM Read / Write Data	0000	RW

PCI V2X Registers

Offset	PCI V2X Control	Default	Acc
71-70	V2X_Base	0000	RW
73-72	V2X_Limit	0000	RW
74	V2X Control	01	RW
75	V2X Mode Delay Control	C0	RW
78	Primary Channel Transport Status I	01	RO
79	Primary Channel Transport Status II	00	RO
7A	Sec Channel Transport Status I	01	RO
7B	Sec Channel Transport Status II	00	RO
7C	Internal PHY Status	00	RO
7D	External PHY Status	00	RO
80	Pri Channel Device Mode Status	00	RO
81	Sec Channel Device Mode Status	00	RO
8B-88	Primary Channel SG Base Address	00000000	RO
8F-8C	Secondary Channel SG Base Addr	00000000	RO

BIST FIS Registers

Offset	BIST FIS Control	Default	Acc
93-90	BIST FIS Control I	00000000	RW
97-94	BIST FIS Control II	00000000	RW
98	BIST FIS Control III	00	RW
99	BIST Command	00	RW

SStatus, SError and SControl Registers

Offset	Status Control	Default	Acc
3-0	SStatus Register	00000000	RO
7-4	SErrror Register	00000000	RWC
8	SControl Registers	00000310	RW

Note: The base addresses are determined by Rx27-24.

Parallel-ATA Function 1 Registers
Configuration Header Registers

Offset	Parallel-ATA Function 0	Default	Acc
A0	Chip Enable	03	RW
A1	IDE Configuration I	C0	RW
A2	IDE Configuration II	81	RW
A3	FIFO Threshold Control	35	RW
A4	Miscellaneous Control I	08	RW
A5	Miscellaneous Control II	35	RW
A6	Miscellaneous Control III	03	RW
AA	Primary IDE Drive #1 Timing Ctrl	A8	RW
AB	Primary IDE Drive #0 Timing Ctrl	A8	RW
AC	IDE Address Setup Time	FF	RW
AD	-reserved-	00	RO
AE	-reserved-	B6	RO
AF	Primary IDE Non-1F0 Port Access Timing	B6	RW
B0-B1	-reserved-	0F	RO
B2	Primary IDE Drive#1 UltraDMA Timing Ctrl	0F	RW
B3	Primary IDE Drive#0 UltraDMA Timing Ctrl	0F	RW
B4	Revision	2C	RW
B8	PLL Control / Test Mode Enable	00	RW
B9	PATA Pad Slew Rate Control	00	RW
BA	DRVRST / Clock Gate Enable / Bus Tri-State Control	04	RW
C0-C1	Primary IDE Sector Size	0200	RW
C8-C9	-reserved-	0200	RO
D0	Primary IDE Status	02	RO
D1	Primary Interrupt Gating	01	RW
D2	PATA Test	00	RW

Register Descriptions

Serial ATA Function 0 Registers

Bridge Configuration Header Registers

Offset 1-0 - Vendor ID = 1106h.....RO

Offset 3-2 - Device ID = 3249h.....RO

Offset 5-4 – PCI Command (0000h).....RW

- 15-10 Reserved RO, always reads 0
- 9 Enabled Fast Back-to-Back def = 0
- 8 System Error Response def = 0
- 7 Address Stepping def = 0
- 6 Parity Error Response..... def = 0
- 5 Reserved RO, always reads 0
- 4 Memory Write and Invalid RO
- 3 Respond to Special Cycles..... RO
- 2 Bus Master..... def = 0
- 1 Memory Space..... def = 0
- 0 Enabled I/O Space Access def = 0

Offset 7-6 – PCI Status (0290h)RW

- 15 Detect Parity Error..... def = 0
- 14 Signaled System Error def = 0
- 13 Received Master Abort def = 0
- 12 Received Target Abort Signal..... def = 0
- 11 Signal Target Abort..... RO, fixed at 0
- 10-9 DEVSEL Timing..... RO, fixed at 01
- 8 Bus Master Parity Err Assertion..... def = 0
- 7 Fast Back to Back Capability RO, fixed at 1
- 6-5 Reserved RO, fixed at 0
- 4 Power Management Capability RO, fixed at 1
- 3-0 Reserved RO, fixed at 0

Offset 8 - Revision ID (80h).....RO

Offset 9 – Programming Interface (8Fh)RO

- 7 Master IDE Device..... def = 1
- 6-4 Fixed at 0 fixed at 0
- 3 Secondary Programmable Indicator..... def = 1
- 2 Secondary Operating Mode
 - 0 Compatible Mode
 - 1 Native Modedefault
- 1 Primary Programmable Indicator def =1
- 0 Primary Operating Mode
 - 0 Compatible Mode
 - 1 Native Modedefault

Offset A – Sub Class (04h)..... RO

- 7-0 Sub Class
 - 01 IDE Controller
 - 04 RAID Controller

Offset B – Base Class (01h)..... RO

- 7-0 Mass Storage Controller.....default = 01h

Offset C – Cache Line Size (00h)..... RO

- 7-0 Fixed at 0.....default =00h

Offset D – Latency Timer (20h) RW

- 7-4 Latency Timer default = 2
- 3-0 Fixed to 0..... RO, default = 0

Offset E – Header Type (00h)..... RO

- 7 Multiple Function Device
- 6-0 Fixed at 0

Offset F – Fixed at 0 (00h) RO

Offset 13-10 – S-ATA Primary Data / Command, Control / Status Base (AF0h)..... RW

- 31-16 Must be 0..... RO
- 15-4 Port AddressRW
- 3-0 Default = 0001b..... RO

A 16 byte IO address space
I/O offset 0~7: data / command ports
I/O offset 8~b: control / status ports

Offset 17-14 – S-ATA Secondary Data / Command, Control / Status Base (A70h) RW

- 31-16 Must be 0..... RO
- 15-4 Port AddressRW
- 3-0 Default = 0001b..... RO

A 16 byte IO address space (only the 3rd byte is active)
I/O offset 0~7: data / command ports
I/O offset 8~b: control / status ports

Offset 1B-18 – PATA Data / Command, Control / Status Base (1F0h)..... RW

- 31-16 Must be 0..... RO
- 15-4 Port AddressRW
- 3-0 Default = 0001b..... RO

A 16 byte IO address space
I/O offset 0~7: data / command ports
I/O offset 8~b: control / status ports

Offset 1F-1C – Reserved Data / Command, Control /
Status Base (170h).....RW

- 31-16 **Must be 0** RO
- 15-4 **Port Address**..... RW
- 3-0 **Default = 0001b**..... RO

A 16 byte IO address space

I/O offset 0~7: data / command ports

I/O offset 8~b: control / status ports

Offset 23-20 – Bus Master Mode Base Add (CC00h)RW

- 31-16 **Must be 0** RO
- 15-5 **Port Address**..... RW
- 4-0 **Default = 00001b**..... RO

A 32 byte IO address space, supports up to 4 bus masters

I/O offset 0~7: 1st channel usage

I/O offset 8~15: 2nd channel usage

I/O offset 16~23 3rd channel usage

I/O offset 24~31: 4th channel usage

Offset 27-24 – S-ATA Ctrl / Status Base Add (8C00h)..RW

- 31-16 **Must be 0** RW
- 15-7 **Port Address**..... RW
- 6-0 **Default = 0001b**..... RO

A 128 byte (2 S-ATA ports) IO address space

offset 00~63: S-ATA1 (1st S-ATA port)

offset 64~127: S-ATA2 (2nd S-ATA port)

Offset 2F-2C – Sub System IDRO

- 31-16 **Sub System ID**..... default = 3249h
- 15-0 **Sub System Vendor ID**..... default = 1106h

Offset 33-30 – Expansion ROM BaseRW

- 31-16 **Expansion ROM Base Address**..... default = 0
- 15-14 **W {11} & R to be 00:64K**
- W {11} & R to be 10:32K**
- W {11} & R to be 11:16K**..... default = 0
- 13-11 **Fixed at 0** RO
- 10-1 **Fixed at 0** RO
- 0 **Expansion ROM Enable** default = 0

If write all 1 to [31:11] and read back the value of all 0,
then no ROM exists.

Offset 34 – PCI Power Mgmt Capabilities PointerRO

- 7-0 **PCI Power Mgmt Capabilities Pointer** ... def = E0h

Offset 3C – Interrupt LineRW

- 7-4 **Interrupt Line Control**..... default = 0
- 3-0 **If [7:4] is 1111b, route to IRQ0, others are decoded to IRQ0 ~ IRQ15**..... default = D

Offset 3D – Interrupt Pin (01h)RO

Use INTA.

Offset 40 – S-ATA Channel Enable (03h) RW

- 7-4 **CHIPID** RO, default = 0
- 3-2 **Reserved**always reads 0
- 1 **S-ATA Primary Channel Enable**.....default = 1
- 0 **S-ATA Secondary Channel Enable**default = 1

Offset 41 – S-ATA Interrupt Gating (03h)..... RW

- 7-4 **Reserved**def = 0
- 3 **Enable PERR Check**.....def = 0
- 2 **Enable SERR Check**def = 0
- 1 **Enable Primary Channel Interrupt Gating**.def = 1
- 0 **Enable Secondary Channel Interrupt Gating**def = 1

Offset 42 –Native Mode Enable (F1h) RW

- 7 **Primary Channel IO Native Mode Enable**...def = 1
- 6 **Secondary Channel IO Native Mode Enable**def = 1
- 5 **Primary Channel Interrupt Native Mode Enable**def = 1
- 4 **Secondary Channel Interrupt Native Mode Enable**.....def = 1
- 3-2 **Reserved** always reads 0
- 1-0 **DEVSEL Timing** def = 01b

Offset 43 – FIFO Threshold Control (40h).....RW

- 7 **Reserved** def = 0
- 6-4 **Primary Channel Threshold Control**.....100b
- 3 **Reserved** def = 0
- 2-0 **Secondary Channel Threshold Control**
 - 000 Zero Threshold
 - 001 1/8
 - 010 1/4
 - 011 3/8
 - 100 1/2
 - 101 5/8
 - 110 3/4
 - 111 7/8

Offset 44 – Miscellaneous Control I (06h)RW

- 7 **Reserved** def = 0
- 6 **Master Read Cycle IRDY# Wait States**..... def = 0
- 5 **Master Write Cycle IRDY# Wait States**..... def = 0
- 4 **Reserved** def = 0
- 3 **Bus Master IDE Status Register Read Retry**def = 0
- 2 **Change Drive to Clear all FIFO Internal States**
 - def = 1
- 1 **Split 2 Channel Request**..... def = 1
- 0 **Reserved** def = 0

Offset 45 – Miscellaneous Control II (9Fh)RW

- 7 **Sub Class (Rx0A) Write Protect**
 - 0 Rx0A Write Enable
 - 1 Rx0A Write Disable.....default
- 6 **Disable Clock Gating**..... def = 0
- 5 **Enable Latency Timer**..... def = 1
Only When GNT is deasserted (to improve performance).
- 4 **Interrupt Line (Rx3C) Write Protect**
 - 0 Rx3C Write Enable.....default
 - 1 Rx3C Write Disable
- 3 **Enable Memory Read Multiple Command** . def = 1
- 2 **Enable Memory Write and Invalidate Command**
 - def = 1
- 1 **Primary Channel Read DMA Flush Data After Interrupt**..... def = 1
- 0 **Secondary Channel Read DMA Flush Data After Interrupt**..... def = 1

Offset 46 – Miscellaneous Control III (00h)..... RW

- 7 **Reserved**default = 0
- 6 **Improve Master Performance Retry Cycle**..... 0
- 5 **Enable IRQ assertion when device is hot plugged**
 - 0
- 4 **Force S-ATA Master/Slave Selection to Master**... 0
- 3 **Reserved**..... 0
- 2 **Enable PLL Reset in S1 State**.....default = 0
Occurs when external PCI clock is stopped.
- 1 **Improve PIO Performance**
 - 0 On default
 - 1 Off
- 0 **Enable Masking PCI Bus Input Floating Signal (in vector mode and test only)** default = 0

Offset 48 – Internal PHY Wake-up (00h)..... RW

- 7-2 **Reserved** def = 0
- 1 **Internal PHY Port2 Wake-up Request** def = 0
- 0 **Internal PHY Port1 Wake-up Request** def = 0

Offset 49 – Strapping Status..... RW

- 7-2 **Reserved** default = 0
- 1 **Card Bus Mode Indicator**..... default = 0
The value depends on the PDA1 strapping value
1: Card bus mode
0: Normal PCI mode
- 0 **Combo Mode Indicator**..... default = 0
The value depends on the PDA2 strapping value
1: Combo mode
0: Normal function mode

Offset 4E – Internal PHY Error Status Output Enable Control (00h)..... RW

- 7-4 **Reserved** 0
- 3 **Enable Internal PHY Secondary Port Error Status (2) Output to EEDI Pin** 0
- 2 **Enable Internal PHY Secondary Port Error Status (1) Output to EEDI Pin** 0
- 1 **Enable Internal PHY Primary Port Error Status (2) Output to EEDI Pin**..... 0
- 0 **Enable Internal PHY Primary Port Error Status (1) Output to EEDI Pin**..... 0

Offset 4F – Error Status Output Enable Control (00h) RW

- 7 **Output BIST Error Signal to EEDI Pin**..... 0
- 6 **Output Device Mode Error Signal to Output Pin** 0
- 5-1 **Reserved** 0
- 0 **Enable Error Signal Output to EEDI Pin** 0

Transport Registers
Offset 50 – Software Ctrl Power Mode Request (00h) ..RW

- 7-4 **Reserved** def = 0
- 3 **Internal PHY Port2 SLUMBER Request**.... def = 0
- 2 **Internal PHY Port2 PARTIAL Request**..... def = 0
- 1 **Internal PHY Port1 SLUMBER Request**.... def = 0
- 0 **Internal PHY Port1 PARTIAL Request**..... def = 0

The internal request is triggered by rising edge of each bit.

Offset 51 – Hardware Ctrl Power Mode (00h).....RW

- 7 **Enable Change Drive and let Idle Device Enter Power Mode**..... default = 0
- 6 **Change Drive Power Mode Selection for Idle Device**
 - 0 **Partial**.....default
 - 1 **Slumber**
- 5 **Reserved**always reads 0
- 4 **Enter to Slumber Process (Item2) Disabled** def = 0
- 3 **Enter to Partial Process (Item1) Disabled** ... def = 0
- 2-0 **PWRCKSEL**
 - 000 **T = t**.....default
 - 001 **T = 2t**
 - ...
 1. Power Mode Control Process: Partial will be requested if transport idle for at least 2T.
 2. Slumber will be requested if transport layer idle for at least 10 T. t = 0.425s

Offset 52 – Transport Miscellaneous Control (00h)RW

- 7 **Reserved** always reads 0
- 6 **Transport Issue Early Request to Link to improve Performance**..... default = 0
- 5 **Reserved** default = 0
- 4 **Single Data FIS Transmission** default = 0
Allow over 8k bytes.
- 3 **BIST FIS**..... default = 0
Controller can accept BIST FIS when behaves as a device (Rx53[1:0] are set). This bit is set only for controller to control BIST FIS self-test.
- 2 **S-ATA Flow Control Water Flag**
 - 1 **FFF0 threshold** (the value is based on RX43)
 - 0 **32DW**.....default
- 1 **COMRESET Will reset both master / slave device (test mode only)** default = 0
- 0 **Reset Shadow Register (test mode only)** default = 0

Offset 53 – Slave Mode Testing (00h) RW

- 7 **SLVSMEMRB**def = 0
Write “1” to trigger slave mode memory read based on the address specified in Rx90 ~ Rx93.
Read value indicates memory read cycle is busy now.
- 6 **SLVSMEMRA**.....def = 0
Write “1” to trigger slave mode memory read based on the address specified in Rx90 ~ Rx93.
Read value indicates memory read cycle is busy now.
- 5 **Secondary Channel CRC Error Status** RO, def = 0
- 4 **Primary Channel CRC Error Status**.... RO, def = 0
- 3 **Secondary Channel Slave Mode Simulation** def = 0
Simulation continues when handshake error occurs (but always stop at CRC error).
- 2 **Primary Channel Slave Mode Simulation**.... def = 0
Simulation continues when handshake error occurs (but always stop at CRC error).
- 1 **Secondary Channel Behaves as Device Controller**def = 0
- 0 **Primary Channel Behaves as Device Controller**def = 0

LINK Registers
Offset 55 – Internal PHY Look Back Test (00h).....RW

- 7-2 Reserved default = 0
- 1 Force Internal PHY Secondary Port as Device Mode (test only) default = 0
- 0 Force Internal PHY First Port as Device Mode (test only) default = 0

Offset 56 – Internal PHY S-ATA LINK Control (00h) .RW

- 7 Reserved def = 0
- 6 Disable RX Scrambler def = 0
- 5 Disable TX Scrambler def = 0
- 4 Disable ALIGN Primitive Transmission def = 0
- 3 Disable CONT Primitive Transmission def = 0
- 2 Enable Continue Primitive after ALIGN def = 0
- 1 Double OOB Burst Number (6 to 12) def = 0
- 0 Disable S-ATA LINK Dynamic Clock Gating def = 0

PHY Registers
Offset 58 – Internal PHY Test Mode Control (00h)..... RW

- 7-4 PHY Test Mode Select default = 0
- 3-2 Reserved default = 0
- 1 Internal Loopback Enable default = 0
- 0 PHY Test Mode Enable default = 0

Offset 59 – Test Pattern Repeat Number (10h) RW

- 7-0 Test Pattern Repeat Number default = 10h

Offset 5A – Internal PHY Control (10h)..... RW

- 7 Reserved def = 0
- 6 Bypass Oscillator def = 0
- 5 OSC Latch up Test Control def = 0
- 4 OOB Signal Select
 - 0 AFE
 - 1 Digital default
- 3 Reserved def = 0
- 2 TxReady Timer Speed up (simulation only) def = 0
- 1 Bailout Mode Test Enable def = 0
- 0 Force PHY Ready (simulation only) def = 0

Offset 5C – Internal PHY Control (05h)..... RW

- 7-6 Reserved default = 0
- 5 CDR Bandwidth Select Bit 1 default = 0
- 4 CDR Bandwidth Select Bit 0 default = 0
- 3 OOB2 Current Control Bit 1 default = 0
- 2 OOB2 Current Control Bit 0 default = 1
- 1 OOB1 Current Control Bit 1 default = 0
- 0 OOB1 Current Control Bit 0 default = 1

Offset 5D – PHY Test Mode Control (00h)..... RW

- 7 Enable S-ATA PLL Testing Mode default = 0
- 6-5 Reserved always reads 0
- 4 Enable Test PIN Data Output default = 0
- 3 Select External PHY Signals default = 0
- 2 Select Secondary Port Signals default = 0
- 1 Select 10B Receive Signals default = 0
- 0 Select 8B Transmit Signals default = 0

Offset 5E – S-ATA Internal PHY Pad Control (00h).... RW

- 7 VCOMP Internal Latch Ctrl Status default = 0
- 6-4 VCOMP Output (only when bit 3 = 0) ... default = 0
- 3 Adjust VCOMP Manually default = 0
- 2-0 VCOMP Control default = 0

RAMBIST Registers

<u>Offset 5F – RAMBIST (00h).....RW</u>	
7-6	Reserved always reads 0
5	Secondary RAMBIST Error Status..... RO, def = 0
4	Trigger Secondary RAMBIST/Busy Status def = 0
3-2	Reserved always reads = 0
1	Primary RAMBIST Error Status..... RO, def = 0
0	Trigger Primary RAMBIST/Busy Status def = 0

BROM Registers

<u>Offset 63-60 – Boot ROM Address (000000h)..... RW</u>	
<u>Offset 67-64 – Boot ROM Read / Write Data (000000h)RW</u>	
<u>Offset 68 – BROM Access Control..... RW</u>	
7	Trigger BROM Data Write default = 0 Read value reflects the busy status of BROM access.
6	BROM Write default = 0
5-4	BROM Size Indicator
	00 64K default
	01 32K
	10 16K
	11 No BROM Device
3-0	BROM Access Byte Enable default = 0
<u>Offset 69 – BROM Error Status (00h)..... RO</u>	
7	BROM Error Status..... RO, default = 0
6-0	Reserved

EEPROM Registers
Offset 6C – EEPROM Access Control (00h)RW

- 7 **EEPROM Operation Start / Ready Status**.. def = 0
Write “1” to this bit triggers EEPROM access operation. Read this bit shows the operation status.
- 6 **EEPROM Read / Write Control**
 - 0 Readdefault
 - 1 Write
- 5-0 **EEPROM Access Address (word based)** def = 0
EEPROM Size: 128 bytes / 64 words.

Offset 6F-6E – EEPROM Read / Write Data (0000h) ...RW

- 15-8 **Offset of Configuration Registers.....** default = 0
 - 7-0 **Content**
- Special pattern:
- 15-0 **16’hFFFF indicates EEPROM Data End**
(Data line is pulled up.)
 - 15-8 **8’h0 indicates Change Function Number**
 - 7-0 **Indicates Function Number if [15:8] = 8’h0**

PCI V2X Registers
Offset 71-70 – V2X Base RW

- 15-0 **V2X Mode Memory Address Base.....**def = 0000h

Offset 73-72 – V2X Limit..... RW

- 15-0 **V2X Mode Memory Address Limit**def = 0000h

Offset 74 – V2X Control (01h)..... RW

- 7-3 **Reserved** default = 0
- 2 **Write 1 to enter V2X Mode** default = 0
- 1 **Active REQ** default = 0
Whenever this bit is set, REQ of the device is active. Thus the bridge can distinguish this device’s REQ-GNT pair from the others.
- 0 **V2X Transaction Acceptance**
 - 0 Bridge cannot accept V2X transactions
 - 1 Bridge can accept V2X transactions..... **default**

Offset 75 – V2X Mode Delay Control (C0h) RW

- 7 **PCI Pad Driving Strength Control**
 - Low driving.....0
 - High driving **default = 1**
- 6 **PCI Pad Slew Rate Control**
 - Low slew rate **default = 1**
 - High slew rate0
- 5-4 **V2X Mode Output DataDelay Selection.....** def = 0
- 3-2 **V2X Mode Output Strobe Delay Select.....** def = 0
- 1-0 **V2X Mode AD Bus Input Delay Select.....** def = 0

Offset 78 – Primary Channel Transport Status I (01h)..RO

- 7-5 Fixed at 0
- 4 Primary Channel DMA Read Device Cycle Active
..... def = 0
- 3 Primary Channel DMA Write Device Cycle Active
..... def = 0
- 2 Primary Channel SG Operation Active..... def = 0
- 1 Primary Channel Interrupt Status..... def = 0
- 0 Primary Channel FIFO Empty Status..... def = 1

Offset 79 – Primary Channel Transport Status II (00h) RO

- 7-5 Reservedalways reads 0
- 4 Primary Channel Slave Drive Select..... def = 0
- 3 Transmit PIO Data Cycle Active..... def = 0
- 2 Receive PIO Data Cycle Active def = 0
- 1 Transmit DMA Data Cycle Active def = 0
- 0 Receive DMA Data Cycle Active def = 0

Offset 7A – Secondary Channel Transport Status I (01h)RO

- 7-5 Reserved always reads 0
- 4 Secondary Channel DMA Read Device Cycle Active def = 0
- 3 Secondary Channel DMA Write Device Cycle Active def = 0
- 2 Secondary Channel SG Operation Active ... def = 0
- 1 Secondary Channel Interrupt Status def = 0
- 0 Secondary Channel FIFO Empty Status def = 1

Offset 7B – Secondary Channel Transport Status II (00h).....RO

- 7-5 Reservedalways reads 0
- 4 Primary Channel Slave Drive Select..... def = 0
- 3 Transmit PIO Data Cycle Active..... def = 0
- 2 Receive PIO Data Cycle Active def = 0
- 1 Transmit DMA Data Cycle Active def = 0
- 0 Receive DMA Data Cycle Active def = 0

Offset 7C – Internal PHY Status..... RO

- 7-6 Reserveddefault = 0
- 5 Port2 Auto Check Error Reportdefault = 0
- 4 Port2 Squelch Detector Output
- 3-2 Reserveddefault = 0
- 1 Port1 Auto Check Error Reportdefault = 0
- 0 Port1 Squelch Detector Output

Offset 7D – External PHY Status (00h)..... RO

- 7-4 Reserveddef = 0
- 3 Internal PHY Port2 Receive COMINITdef = 0
- 2 Internal PHY Port2 Receive COMWAKE ..def = 0
- 1 Internal PHY Port1 Receive COMINITdef = 0
- 0 Internal PHY Port1 Receive COMWAKE ..def = 0

Offset 80 – Primary Channel Device Mode Status RO

- 7-0 Primary Channel Parsing FIS Number when in Device modedefault = 0

Offset 81 – Secondary Channel Device Mode Status..... RO

- 7-0 Secondary Channel Parsing FIS Number when in Device mode.....default = 0

Offset 8B-88 – Primary Channel SG Base Address..... RO
Offset 8F-8C – Secondary Channel SG Base Address ... RO

BIST FIS Registers
Offset 93-90 – BIST FIS Control I (00000000h).....RW
32-0 BIST FIS Control I

This register is for the following purposes:

- 1) BIST FIS first DW content
- 2) RAMBIST test pattern first DW content
- 3) Device mode bitmap table address

Offset 97-94 – BIST FIS Control II (00000000h)RW
32-0 BIST FIS Control II

This register is for the following purposes:

- 1) BIST FIS secondary DW content
- 2) RAMBIST test pattern secondary DW content

Offset 98 – BIST FIS Control III (00h).....RW

- 7 **Far End Transmit Only Mode**..... default = 0
- 6 **Bypass Transmit ALIGN Primitive** default = 0
- 5 **Bypass Scramble** default = 0
- 4 **Far End Retime Loop Back** default = 0
- 3 **Far End Analog (AFE) Loop Back (not supported)**
- 2 **Primitive Bit (not supported)**..... default = 0
- 1 **Reserved** default = 0
- 0 **Vendor Specific Test Mode**..... default = 0

Offset 99 – BIST Command (00h).....RW

- 7 **Secondary Channel in Receive Loop Back Mode**
.....RO, default = 0
- 6 **Primary Channel in Receive Loop Back Mode**
.....RO, default = 0
- 5 **Secondary Channel in Transmit Loop Back Mode**
.....RO, default = 0
- 4 **Primary Channel in Transmit Loop Back Mode**
.....RO, default = 0
- 3 **Secondary Channel BIST Error Status**
.....RO, default = 0
- 2 **Primary Channel BIST Error Status**
.....RO, default = 0
- 1 **Secondary Channel BIST FIS Start / Busy Status**
Write “1” to this bit triggers BIST FIS Far-End loop back mode. Read “1” to reflect the BIST busy status.
..... default = 0
- 0 **Primary Channel BIST FIS Start / Busy Status**
Write “1” to this bit triggers BIST FIS Far-End loop back mode. Read “1” to reflect the BIST busy status.
..... default = 0

SStatus, SError and SControl Registers

Offset 3-0 – SStatus (00000000h).....RO

- 31-12 Fixed at 0 always reads 0**
- 11-8 IPM**
Indicates the current interface power management.
0000 Device not present or communication not established
0001 Interface in active state
0010 Interface in PARTIAL power mgmt state
0110 Interface in SLUMBER power mgmt state
- 7-4 SPD**
Indicates the negotiated interface communication speed established.
0000 No negotiated speed (device not present or communication not established)
0001 Generation 1 communication rate negotiated
- 3-0 DET**
Indicates the interface device detection and PHY state.
0000 No device detected and PHY communication not established
0001 Device presence detected but PHY communication not established
0011 Device presence detected and PHY communication established
0100 PHY in offline mode as a result of interface disabled or running in a BIST loopback mode

Offset 7-4 – SError (00000000h).....RWC

- 31-26 Reserved always reads 0**
- 25 Unrecognized FIS Type default = 0**
- 24 Transport State Transition Error default = 0**
- 23 Link Sequence Error default = 0**
- 22 Handshake Error default = 0**
- 21 CRC Error default = 0**
- 20 Disparity Error default = 0**
- 19 10B to 8B Decode Error default = 0**
- 18 Comm Wake Detected default = 0**
- 17 PHY Internal Error default = 0**
- 16 PHY Ready Change default = 0**
- 15-12 Reserved always reads 0**
- 11 Internal Error default = 0**
- 10 Protocol Error default = 0**
- 9 Non-recovered Persistent Communication or Data Integrity Error default = 0**
- 8 Non-recovered Transient Data Integrity Error default = 0**
- 7-2 Reserved always reads 0**
- 1 Recovered Communications Error default = 0**
- 0 Recovered Data Integrity Error default = 0**

Offset B-8 – SControl (00000310h).....RO

- 31-12 Reserved always reads 0**
- 11-8 IPM**
Represents the enabled interface power management states that can be invoked via S-ATA interface power management capabilities.
0000 No interface power mgmt state restrictions
0001 Transitions to the PARTIAL power mgmt state disabled
0010 Transitions to the SLUMBER power mgmt state disabled
0011 Transitions to both the PARTIAL and SLUMBER power mgmt states disabled.....**def**
All other values are reserved.
- 7-4 SPD**
Represents the maximum communication speed that the interface is allowed.
0000 No speed negotiation restrictions
0001 Limit speed negotiation to a rate not greater than Generation 1 communication rate.....**def**
All other values are reserved.
- 3-0 DET**
Controls the host adapter device detection and interface initialization.
0000 No device detection or initialization action requested.....**def**
0001 Perform interface communication initialization sequence to establish communication
0100 Disable the S-ATA interface and put PHY in offline mode
All other values are reserved.

Parallel ATA Function 1 Registers

Offset A0 – IDE Chip Enable (03h).....RW

- 7-4 **Reserved**RO, default = 0
- 3-2 **Reserved** default = 0
- 1 **Primary Channel**
 - 0 Disable
 - 1 Enabledefault
- 0 **Reserved** default = 1

Offset A1 – IDE Configuration I (C0h).....RW

- 7 **Primary IDE Read Prefetch Buffer**
 - 0 Disable
 - 1 Enabledefault
- 6 **Primary IDE Post Write Buffer**
 - 0 Disable
 - 1 Enabledefault
- 5-0 **Reserved**32h

Note: DCS16# source always decodes from BE[3:0]#, no optional bit selected.

Offset A2 –IDE Configuration II (81h).....RW

- 7-2 **Reserved**32h
- 1-0 **DEVSEL# Timing**..... default = 01b

Offset A3 – FIFO Threshold Control (35h)..... RW

- 7-4 **Reserved** 03h
- 3-2 **Primary Channel Threshold**
 - 00 1/4
 - 01 1/2..... default
 - 10 3/4
 - 11 1
- 1-0 **Reserved**default = 01

Offset A4 – Miscellaneous Control I (08h)..... RW

- 7 **Reserved**always reads 0
- 6 **Master Read Cycle IRDY# Wait States**
 - default = 0 (disable)
- 5 **Master Write Cycle IRDY# Wait States**
 - default = 0 (disable)
- 4 **PIO Read Pre-Fetch Byte Counter**
 - 0 Disable
 - 1 Enable default
- 3 **Bus Master IDE Status Register Read Retry**
 - 0 Disable default
 - 1 Enable
- 2 **Packet Command Prefetching**

Determines whether prefetching is enabled for packet commands. Packet commands are commands for ATAPI, which is used for operating devices such as CD-ROM drives.

 - 0 Disable..... default
 - 1 Enable
- 1 **Reserved**always reads 0
- 0 **UltraDMA Host Must Wait for First Transfer Before Termination**
 - 0 Enable. The UltraDMA host must wait until at least the first transfer is completed before it can terminate a transaction default
 - 1 Disable

Offset A5 – Miscellaneous Control II (35h).....RW

- 7 **Reserved** default = 0
- 6 **Reserved** default = 0
- 5 **Enable Latency Timer**
Enable latency timer when PCI grant is unasserted to improve performance,
0 Disable
1 Enable**default**
- 4 **Reserved** default = 0
- 3 **Memory-Read-Multiple Command**
0 Disable
1 Enable**default**
- 2 **Memory-Write-and-Invalidate Command**
0 Disable
1 Enable**default**
- 1 **Force Internal Clock as 100MHz Clock Source**
0 Disabledefault
1 Enable
- 0 **Reserved**always reads 0

Offset A6 – Miscellaneous Control III (03h)RW

- 7 **Primary Channel Read DMA FIFO Flush**
0 Disable
1 Enable**default**
- 6-4 **Reserved**100b
- 3-2 **Fixed at 0** **RO, fixed**
- 1-0 **Reserved** default = 0

Offset AA – Primary IDE Drive #1 Timing Ctrl (A8h).RW

- 7-4 **DIOR# / DIOW# Active Pulse Width**
- 3-0 **DIOR# / DIOW# Recovery Time**

Offset AB – Primary IDE Drive #0 Timing Ctrl (A8h).RW

- 7-4 **DIOR# / DIOW# Active Pulse Width**
- 3-0 **DIOR# / DIOW# Recovery Time**

Offset AC – IDE Address Setup Time (FFh) RW

- 7-6 **Primary Drive #0**
00 1T
01 2T
10 3T
11 4T..... default
- 5-4 **Primary Drive# 1**
- 3-2 **Secondary Drive# 0**
- 1-0 **Secondary Drive# 1**

Offset AF – Primary IDE Non-1F0 Port Access Timing (B6h) RW

- 7-4 **DIOR# / DIOW# Active Pulse Width**..... def = 0Bh
- 3-0 **DIOR# / DIOW# Recovery Time**.....def = 06h

The above fields define the primary and secondary channel DIOR# and DIOW# active pulse widths and recovery times when accessing non-data ports. The times are defined in terms of PCI clocks and the actual value is equal to the value encoded in the field plus one.

Offset B2 – Primary IDE Drive #1 UltraDMA Timing

Ctrl (0Fh).....RW

- 7 Primary Drive#1 UltraDMA Mode Enable Method**
 - 0 Enable by using “Set Feature” Command....def
 - 1 Enable by setting bit [3:0] of this register
- 6 Primary Drive#1 UltraDMA Mode Enable**
 - 0 Disable
 - 1 Enable
- 5 Transfer Mode Status.....RO**
 - 0 DMA or PIO Mode
 - 1 Ultra Mode
- 4 Primary Drive#1 Cabal Type ReportingRO**
- 3-0 Cycle Time**
 - 0 2T
 - 1 3T
 - ...
 - 7 9T
 - ...
 - 15 17T.....default

Offset B3 – Primary IDE Drive #0 UltraDMA Timing

Ctrl (0Fh).....RW

- 7 Primary Drive#0 UltraDMA Mode Enable Method**
 - 0 Enable by using “Set Feature” Command....def
 - 1 Enable by setting bit [3:0] of this register
- 6 Primary Drive#0 UltraDMA Mode Enable**
 - 0 Disable
 - 1 Enable
- 5 Transfer Mode Status.....RO**
 - 0 DMA or PIO Mode
 - 1 Ultra Mode
- 4 Primary Drive#0 Cabal Type ReportingRO**
- 3-0 Cycle Time**
 - 0 2T
 - 1 3T
 - ...
 - 7 9T
 - ...
 - 15 17T.....default

Offset B4 – Revision Register (2Ch) RW

- 7 Enable UltraDMA De-bouncing Circuit def = 0**
- 6 Reserved..... def = 0**
- 5 Improve Prefetch / Port –Write Performance**
 - 0 Enable
 - 1 Disable..... **default**
- 4 Split REQ Change Channel**
 - 0 Disable
 - 1 Enable..... **default**
- 3 Clear Native Mode Interrupt by the Falling edge of Device Interrupt**
 - 0 On default
 - 1 Off
- 2 Change Drive to Clear All FIFO and Internal States**
 - 0 Disable
 - 1 Enable..... **default**
- 1 Reserved.....always reads 0**
- 0 Complete DMA Cycle with Transfer Size less Than FIFO Size**
 - 0 Enable. DMA transfer size is less than the FIFO size default
 - 1 Disable

Offset B8 – PLL Control / Test Mode Enable (00h)..... RW

- 7-6 PLL Input PCICLK Delay Control Bits def = 00**
- 5-4 PLL Input FBCLK Delay Control Bits def = 00**
- 3 Enable PLL Test Mode def = 0**
 - 0 Disable..... default
 - 1 Enable
- 2-0 PLL Test Mode def = 000**

Offset B9 – PATA Pad Slew Rate Control (00h) RW

- 7-6 Primary Channel..... default = 00**
- 5-4 Secondary Channel default = 00**
- 3-0 Fixed at 0.....always reads 0**

Offset BA – DRVST Clock Gate / Bus Tri-State

Control (04h)RW

- 7 Primary Channel Device Reset**
 - 0 Disabledefault
 - 1 Enable
- 6 Secondary Channel Device Reset**
 - 0 Disabledefault
 - 1 Enable
- 5 Enable Clock Gating**
 - 0 Disable
 - 1 Enable Gated Clockdefault
- 4-2 Fixed at 0RO, always reads 0**
- 1 Primary IDE Bus Power-off Enable**
 - 0 Disabledefault
 - 1 Enable
- 0 Secondary IDE Bus Power-off Enable**
 - 0 Disabledefault
 - 1 Enable

Offset C0-C1 – Primary IDE Sector Size (0200h).....RW

- 15-12 ReservedRO, always reads 0**
- 11-0 Number of Bytes Per Sector. def = 200h (512 bytes)**

Offset D0 – Primary IDE Status (02h)..... RO

- 7 Interrupt StatusRO**
- 6 Prefetch Buffer Status.....RO**
- 5 Post Write Buffer Status.....RO**
- 4 DMA Read Prefetch StatusRO**
- 3 DMA Write Pipeline StatusRO**
- 2 S/G Operation CompleteRO**
- 1 FIFO Empty StatusRO**
- 0 External DMA Request StatusRO**

Offset D1 – Primary Interrupt Gating (01h)..... RW

- 7-1 Reservedalways reads 0**
- 0 Interrupt Gating**
 - 0 Disable
 - 1 Enable (IRQ output gated until FIFO empty)
..... default

Offset D2 – PATA Test (00h)..... RW

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit	Comment
T _{STG}	Storage Temperature	-55	125	°C	
T _C	Case Operating Temperature	0	85	°C	
V _{CC}	Power Supply Voltages	3.0	3.6	V	
V _I	Input Voltage	-0.5	V _{CC} + 0.5	V	
V _O	Output Voltage (at any output)	-0.5	V _{CC} + 0.5	V	
V _{ESD}	Electrostatic Discharge		2	kV	Human Body Model

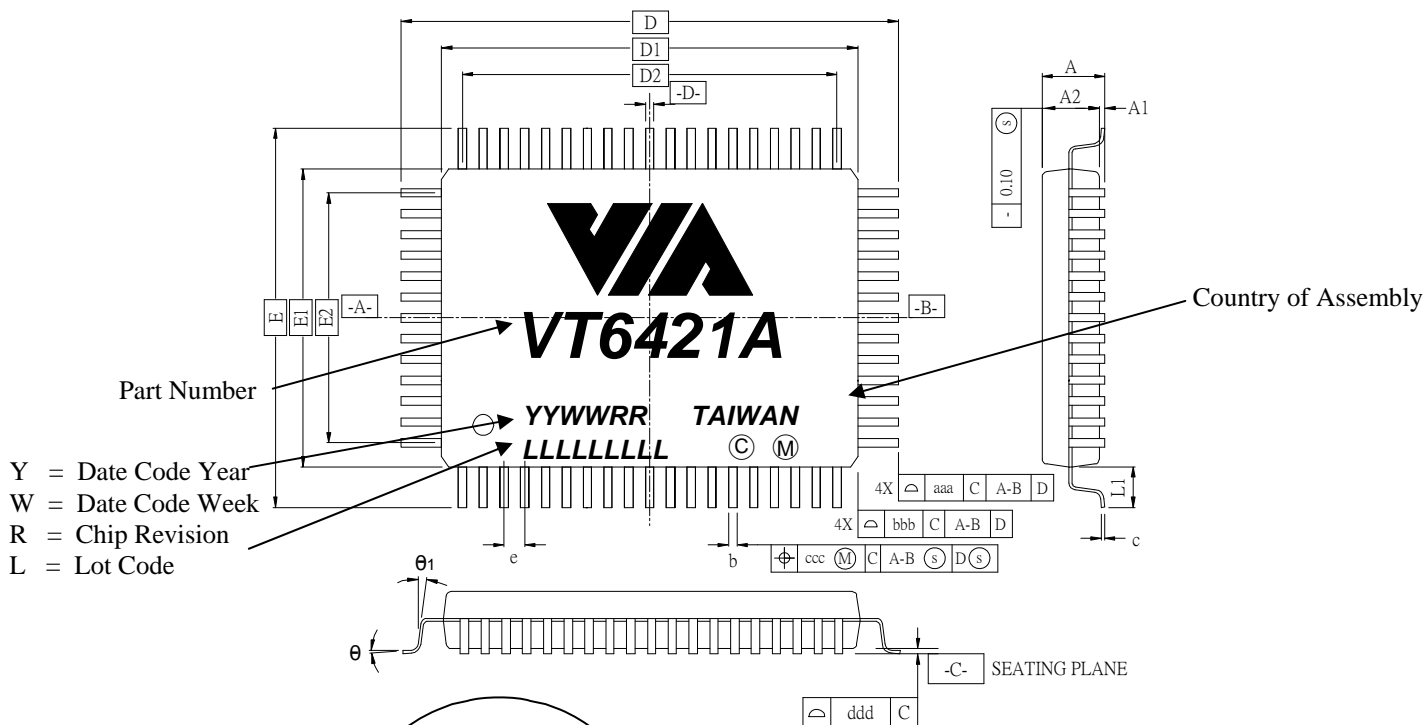
Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Specifications

T_C = 0-55°C, V_{CCPCI} = V_{CCPLL} = 3.3V ± 5%, V_{CC25} = V_{CCOSC} = V_{CCPLLA} = 2.5V ± 5%, GND = 0V

Symbol	Parameter	Min	Max	Unit	Condition
V _{IL}	Input Low Voltage	-0.5	0.8	V	
V _{IH}	Input High Voltage	2.0	V _{CC} + 0.5	V	
V _{OL}	Output Low Voltage	-	0.45	V	I _{OL} = 4.0 mA
V _{OH}	Output High Voltage	2.4	-	V	I _{OH} = 1.0 mA
I _{IL}	Input Leakage	-	±10	μA	0 < V _{IN} < V _{CC}
I _{OZ}	Tristate Leakage Current	-	±20	μA	0.45 < V _{OUT} < V _{CC}

MECHANICAL SPECIFICATIONS



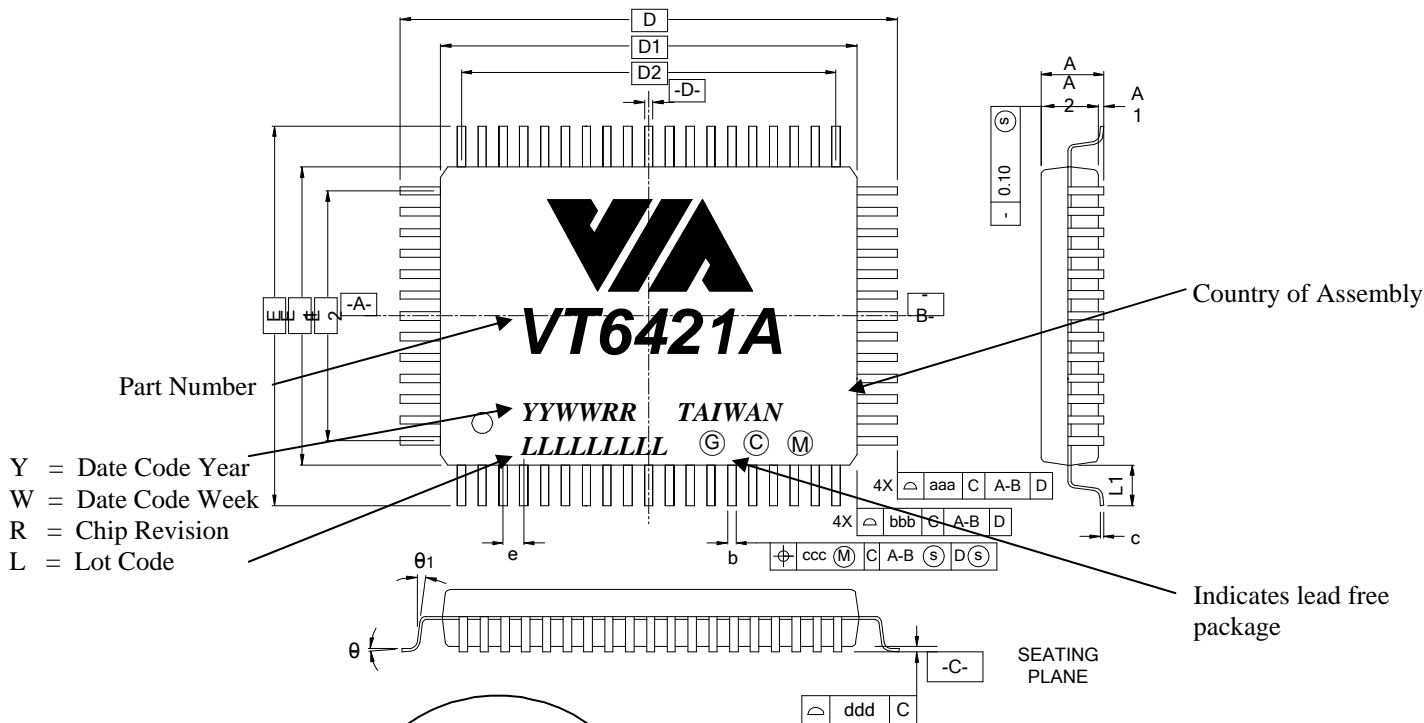
CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	22.00 BASIC			0.866 BASIC		
E	16.00 BASIC			0.630 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E1	14.00 BASIC			0.551 BASIC		
D2	18.50 BASIC			0.728 BASIC		
E2	12.50 BASIC			0.492 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0	3.5	7	0	3.5	7
θ1	0	—	—	0	—	—
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

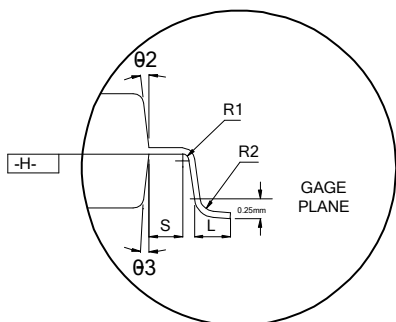
NOTES :

- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 3. Mechanical Specification – 128 Pin LQFP (14X20mm)



Y = Date Code Year
W = Date Code Week
R = Chip Revision
L = Lot Code



NOTES :

- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	22.00 BASIC			0.866 BASIC		
E	16.00 BASIC			0.630 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E1	14.00 BASIC			0.551 BASIC		
D2	18.50 BASIC			0.728 BASIC		
E2	12.50 BASIC			0.492 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
theta	0	3.5	7	0	3.5	7
theta1	0	—	—	0	—	—
theta2	11	12	13	11	12	13
theta3	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 4. Lead-Free Mechanical Specification – 128 Pin LQFP (14X20mm)