

DDR4 SDRAM SODIMM

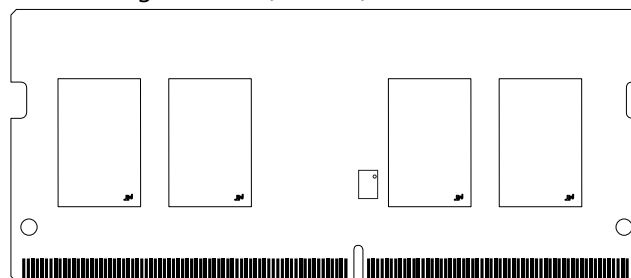
MTA4ATF51264HZ – 4GB

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- 260-pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC4-2666, PC4-2400 and PC4-2133
- 4GB (512 Meg x 64)
- $V_{DD} = 1.20V$ (NOM)
- $V_{PP} = 2.5V$ (NOM)
- $V_{DDSPD} = 2.5V$ (NOM)
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- On-die V_{REFDQ} generation and calibration
- Single-rank
- On-board I²C serial presence-detect (SPD) EEPROM
- 8 internal banks; 2 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control command and address bus

Figure 1: 260-Pin SODIMM (MO-310 R/C C)

Module Height: 30mm (1.181 in)



Options

- Operating temperature
 - Commercial ($0^{\circ}C \leq T_{OPER} \leq 95^{\circ}C$)
- Package
 - 260-pin DIMM (halogen-free)
- Frequency/CAS latency
 - 0.75ns @ CL = 19 (DDR4-2666)
 - 0.83ns @ CL = 17 (DDR4-2400)
 - 0.93ns @ CL = 15 (DDR4-2133)

Marking

None
Z
-2G6
-2G3
-2G1

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)											t_{RCD} (ns)	t_{RP} (ns)	t_{RC} (ns)
		CL = 20, CL = 19	CL = 18	CL = 17	CL = 16	CL = 15	CL = 14	CL = 13	CL = 12	CL = 11	CL = 10	CL = 9			
-2G6	PC4-2666	2666	2666	2400	2133	2133	1866	1866	1600	–	1333	–	14.16	14.16	46.16
-2G4	PC4-2400	–	2400	2400	2400	2133	1866	1866	1600	1600	–	1333	13.32	13.32	45.32
-2G3	PC4-2400	–	2400	2400	2133	2133	1866	1866	1600	1600	1333	–	14.16	14.16	46.16
-2G1	PC4-2133	–	–	–	2133	2133	1866	1866	1600	1600	–	1333	13.5	13.5	46.5

Table 2: Addressing

Parameter	4GB
Row address	64K A[15:0]
Column address	1K A[9:0]
Device bank group address	2 BG0
Device bank address per group	4 BA[1:0]
Device configuration	8Gb (512 Meg x 16), 8 banks
Module rank address	CS0_n

Table 3: Part Numbers and Timing Parameters – 4GB Modules

Base device: MT40A512M16,¹ 8Gb DDR4 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- ^t RCD- ^t RP)
MTA4ATF51264HZ-2G6__	4GB	512 Meg x 64	21.3 GB/s	0.75ns/2666 MT/s	19-19-19
MTA4ATF51264HZ-2G3__	4GB	512 Meg x 64	19.2 GB/s	0.83ns/2400 MT/s	17-17-17
MTA4ATF51264HZ-2G1__	4GB	512 Meg x 64	17.0 GB/s	0.93ns/2133 MT/s	15-15-15

- Notes:
1. The data sheet for the base device can be found on micron.com.
 2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA4ATF51264HZ-2G3B1.



4GB (x64, SR) 260-Pin DDR4 SODIMM Pin Assignments

Pin Assignments

The pin assignment table below is a comprehensive list of all possible pin assignments for DDR4 SODIMM modules. See Functional Block Diagram for pins specific to this module.

Table 4: Pin Assignments

260-Pin DDR4 SODIMM Front								260-Pin DDR4 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V _{SS}	67	DQ29	133	A1	199	DM5_n/ DBI5_n	2	V _{SS}	68	V _{SS}	134	EVENT_n, NF	200	DQ55_t
3	DQ5	69	V _{SS}	135	V _{DD}	201	V _{SS}	4	DQ4	70	DQ24	136	V _{DD}	202	V _{SS}
5	V _{SS}	71	DQ25	137	CK0_t	203	DQ46	6	V _{SS}	72	V _{SS}	138	CK1_t/NF	204	DQ47
7	DQ1	73	V _{SS}	139	CK0_c	205	V _{SS}	8	DQ0	74	DQS3_c	140	CK1_c/NF	206	V _{SS}
9	V _{SS}	75	DM3_n/ DBI3_n	141	V _{DD}	207	DQ42	10	V _{SS}	76	DQS3_t	142	V _{DD}	208	DQ43
11	DQS0_c	77	V _{SS}	143	PARITY	209	V _{SS}	12	DM0_n/ DBI0_n	78	V _{SS}	144	A0	210	V _{SS}
13	DQS0_t	79	DQ30	145	BA1	211	DQ52	14	V _{SS}	80	DQ31	146	A10/AP	212	DQ53
15	V _{SS}	81	V _{SS}	147	V _{DD}	213	V _{SS}	16	DQ6	82	V _{SS}	148	V _{DD}	214	V _{SS}
17	DQ7	83	DQ26	149	CS0_n	215	DQ49	18	V _{SS}	84	DQ27	150	BA0	216	DQ48
19	V _{SS}	85	V _{SS}	151	WE_n/ A14	217	V _{SS}	20	DQ2	86	V _{SS}	152	RAS_n/ A16	218	V _{SS}
21	DQ3	87	CB5/NC	153	V _{DD}	219	DQ56_c	22	V _{SS}	88	CB4/NC	154	V _{DD}	220	DM6_n/ DBI6_n
23	V _{SS}	89	V _{SS}	155	ODT0	221	DQ56_t	24	DQ12	90	V _{SS}	156	CAS_n/ A15	222	V _{SS}
25	DQ13	91	CB1/NC	157	CS1_n/ NC	223	V _{SS}	26	V _{SS}	92	CB0/NC	158	A13	224	DQ54
27	V _{SS}	93	V _{SS}	159	V _{DD}	225	DQ55	28	DQ8	94	V _{SS}	160	V _{DD}	226	V _{SS}
29	DQ9	95	DQS8_c	161	ODT1/ NC	227	V _{SS}	30	V _{SS}	96	DM8_n/ DBI_n/NC	162	C0/ CS2_n/NC	228	DQ50
31	V _{SS}	97	DQS8_t	163	V _{DD}	229	DQ51	32	DQS1_c	98	V _{SS}	164	V _{REFCA}	230	V _{SS}
33	DM1_n/ DBI_n	99	V _{SS}	165	C1, CS3_n, NC	231	V _{SS}	34	DQS1_t	100	CB6/NC	166	SA2	232	DQ60
35	V _{SS}	101	CB2/NC	167	V _{SS}	233	DQ61	36	V _{SS}	102	V _{SS}	168	V _{SS}	234	V _{SS}
37	DQ15	103	V _{SS}	169	DQ37	235	V _{SS}	38	DQ14	104	CB7/NC	170	DQ36	236	DQ57
39	V _{SS}	105	CB3/NC	171	V _{SS}	237	DQ56	40	V _{SS}	106	V _{SS}	172	V _{SS}	238	V _{SS}
41	DQ10	107	V _{SS}	173	DQ33	239	V _{SS}	42	DQ11	108	RESET_n	174	DQ32	240	DQS7_c
43	V _{SS}	109	CKE0	175	V _{SS}	241	DM7_n/ DBI7_n	44	V _{SS}	110	CKE1/ NC	176	V _{SS}	242	DQS7_t
45	DQ21	111	V _{DD}	177	DQS4_c	243	V _{SS}	46	DQ20	112	V _{DD}	178	DM4_n/ DBI4_n	244	V _{SS}
47	V _{SS}	113	BG1	179	DQS4_t	245	DQ62	48	V _{SS}	114	ACT_n	180	V _{SS}	246	DQ63
49	DQ17	115	BG0	181	V _{SS}	247	V _{SS}	50	DQ16	116	ALERT_n	182	DQ39	248	V _{SS}
51	V _{SS}	117	V _{DD}	183	DQ38	249	DQ58	52	V _{SS}	118	V _{DD}	184	V _{SS}	250	DQ59
53	DQS2_c	119	A12	185	V _{SS}	251	V _{SS}	54	DM2_n/ DBI2_n	120	A11	186	DQ35	252	V _{SS}
55	DQS2_t	121	A9	187	DQ34	253	SCL	56	V _{SS}	122	A7	188	V _{SS}	254	SDA
57	V _{SS}	123	V _{DD}	189	V _{SS}	255	V _{DDSPD}	58	DQ22	124	V _{DD}	190	DQ45	256	SA0



4GB (x64, SR) 260-Pin DDR4 SODIMM Pin Assignments

Table 4: Pin Assignments (Continued)

260-Pin DDR4 SODIMM Front								260-Pin DDR4 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
59	DQ23	125	A8	191	DQ44	257	V _{PP}	60	V _{SS}	126	A5	192	V _{SS}	258	V _{TT}
61	V _{SS}	127	A6	193	V _{SS}	259	V _{PP}	62	DQ18	128	A4	194	DQ41	260	SA1
63	DQ19	129	V _{DD}	195	DQ40	–	–	64	V _{SS}	130	V _{DD}	196	V _{SS}	–	–
65	V _{SS}	131	A3	197	V _{SS}	–	–	66	DQ28	132	A2	198	DQS5_c	–	–

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for DDR4 modules. All pins listed may not be supported on this module. See Functional Block Diagram for pins specific to this module.

Table 5: Pin Descriptions

Symbol	Type	Description
Ax	Input	Address inputs: Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands in order to select one location out of the memory array in the respective bank (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A17 is only defined for x4 SDRAM.
A10/AP	Input	Auto precharge: A10 is sampled during READ and WRITE commands to determine whether an auto precharge should be performed on the accessed bank after a READ or WRITE operation (HIGH = auto precharge; LOW = no auto precharge). A10 is sampled during a PRECHARGE command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	Burst chop: A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH = no burst chop; LOW = burst-chopped). See Command Truth Table in the DDR4 component data sheet.
ACT_n	Input	Command input: ACT_n defines the ACTIVATE command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 are considered as row address A16, A15, and A14. See Command Truth Table.
BAX	Input	Bank address inputs: Define the bank (with a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command.
BGx	Input	Bank group address inputs: Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16-based SDRAM only has BG0.
C0, C1, C2 (RDIMM/LRDIMM only)	Input	Chip ID: These inputs are used only when devices are stacked; that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using through-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP package, which uses CS1_n, CKE1, and ODT1 to control the second die. All other stack configurations, such as a 4H or 8H, are assumed to be single-load (master/slave) type configurations where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code.
CKx_t CKx_c	Input	Clock: Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.
CKEx	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After V _{REFCA} has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during self refresh.
CSx_n	Input	Chip select: All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code (CS2_n and CS3_n are not used on UDIMMs).

Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
ODTx	Input	On-die termination: ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (R_{TT}) is applied only to each DQ, DQS _t , DQS _c , DM _n /DBI _n /TDQS _t , and TDQS _c signal for x4 and x8 configurations (when the TDQS function is enabled via the mode register). For the x16 configuration, R_{TT} is applied to each DQ, DQSU _t , DQSU _c , DQSL _t , DQSL _c , UDM _n , and LDM _n signal. The ODT pin will be ignored if the mode registers are programmed to disable R_{TT} .
PARITY	Input	Parity for command and address: This function can be enabled or disabled via the mode register. When enabled in MR5, the DRAM calculates parity with ACT _n , RAS _n /A16, CAS _n /A15, WE _n /A14, BG[1:0], BA[1:0], A[16:0]. Input parity should be maintained at the rising edge of the clock and at the same time as command and address with CS _n LOW.
RAS _n /A16 CAS _n /A15 WE _n /A14	Input	Command inputs: RAS _n /A16, CAS _n /A15, and WE _n /A14 (along with CS _n) define the command and/or address being entered and have multiple functions. For example, for activation with ACT _n LOW, these are addresses like A16, A15, and A14, but for a non-activation command with ACT _n HIGH, these are command pins for READ, WRITE, and other commands defined in Command Truth Table.
RESET _n	CMOS Input	Active LOW asynchronous reset: Reset is active when RESET _n is LOW and inactive when RESET _n is HIGH. RESET _n must be HIGH during normal operation.
SAX	Input	Serial address inputs: Used to configure the temperature sensor/SPD EEPROM address range on the I ² C bus.
SCL	Input	Serial clock for temperature sensor/SPD EEPROM: Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I ² C bus.
DQx, CBx	I/O	Data input/output and check bit input/output: Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If cyclic redundancy checksum (CRC) is enabled via the mode register, the CRC code is added at the end of the data burst. Any one or all of DQ0, DQ1, DQ2, or DQ3 may be used for monitoring of internal V_{REF} level during test via mode register setting MR[4] A[4] = HIGH; training times change when enabled.
DM _n /DBI _n / TDQS _t (DMU _n , DBIU _n), (DML _n / DBIL _n)	I/O	Input data mask and data bus inversion: DM _n is an input mask signal for write data. Input data is masked when DM _n is sampled LOW coincident with that input data during a write access. DM _n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI _n is an input/output identifying whether to store/output the true or inverted data. If DBI _n is LOW, the data will be stored/output after inversion inside the DDR4 device and not inverted if DBI _n is HIGH. TDQS is only supported in x8 SDRAM configurations (TDQS is not valid for UDIMMs).
SDA	I/O	Serial Data: Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device.
DQS _t DQS _c DQSU _t DQSU _c DQSL _t DQSL _c	I/O	Data strobe: Output with read data, input with write data. Edge-aligned with read data, centered-aligned with write data. For x16 configurations, DQSL corresponds to the data on DQ[7:0], and DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
ALERT _n	Output	Alert output: Possesses functions such as CRC error flag and command and address parity error flag as output signal. If a CRC error occurs, ALERT _n goes LOW for the period time interval and returns HIGH. If an error occurs during a command address parity check, ALERT _n goes LOW until the on-going DRAM internal recovery transaction is complete. During connectivity test mode, this pin functions as an input. Use of this signal is system-dependent. If not connected as signal, ALERT _n pin must be connected to V_{DD} on DIMMs.
EVENT _n	Output	Temperature event: The EVENT _n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.

Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
TDQS_t TDQS_c (x8 DRAM-based RDIMM only)	Output	Termination data strobe: When enabled via the mode register, the DRAM device enables the same R_{TT} termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin provides the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations. DM, DBI, and TDQS are a shared pin and are enabled/disabled by mode register settings. For more information about TDQS, see the DDR4 DRAM component data sheet (TDQS_t and TDQS_c are not valid for UDIMMs).
V _{DD}	Supply	Module power supply: 1.2V (TYP).
V _{PP}	Supply	DRAM activating power supply: 2.5V –0.125V / +0.250V.
V _{REFCA}	Supply	Reference voltage for control, command, and address pins.
V _{SS}	Supply	Ground.
V _{TT}	Supply	Power supply for termination of address, command, and control V _{DD} /2.
V _{DDSPD}	Supply	Power supply used to power the I ² C bus for SPD.
RFU	–	Reserved for future use.
NC	–	No connect: No internal electrical connection is present.
NF	–	No function: May have internal connection present, but has no function.

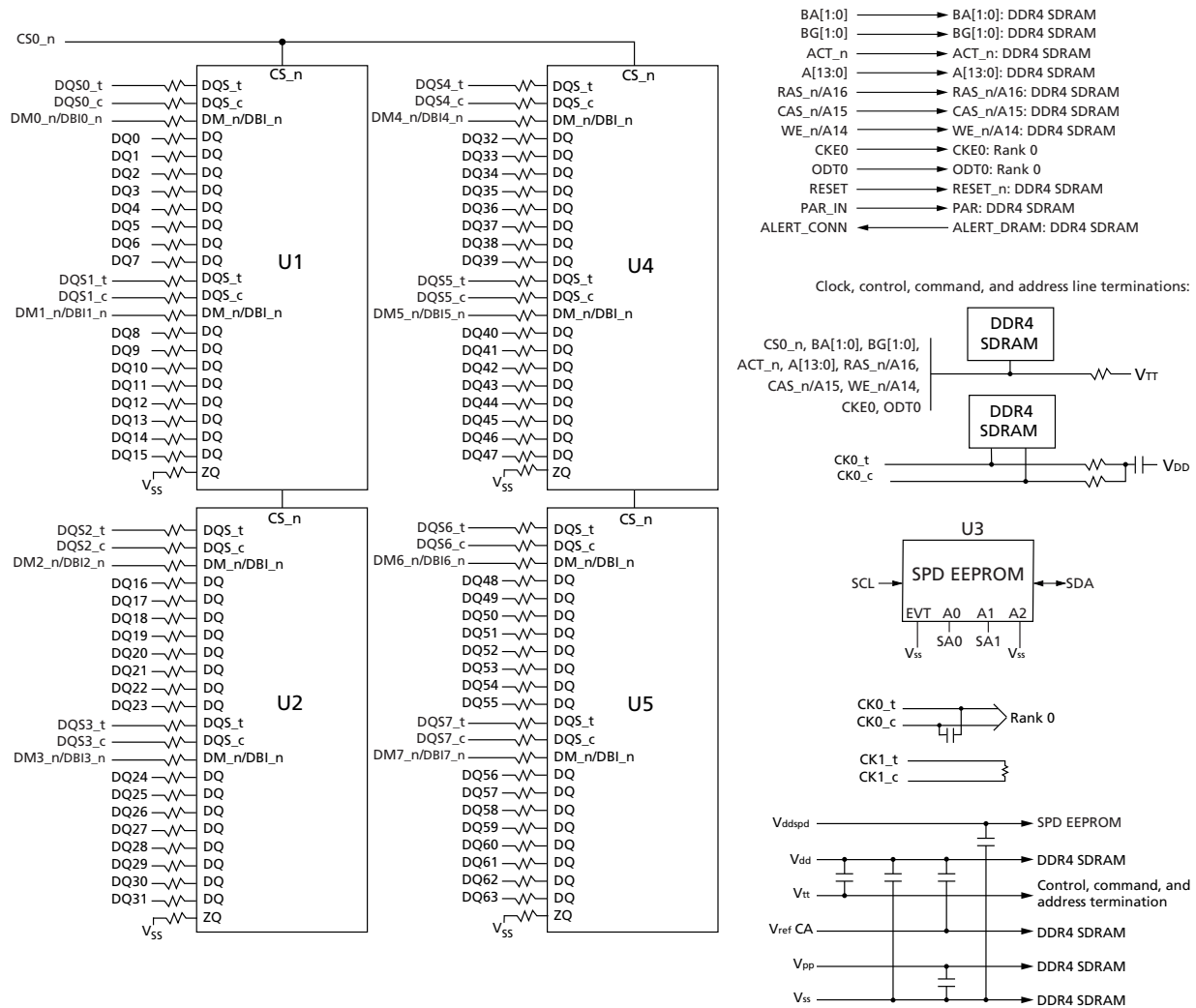
DQ Map

Table 6: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	00	3	21	U2	00	19	63
	01	1	7		01	17	49
	02	2	20		02	18	62
	03	0	8		03	16	50
	04	7	17		04	23	59
	05	5	3		05	21	45
	06	6	16		06	22	58
	07	4	4		07	20	46
	08	10	41		08	26	83
	09	8	28		09	24	70
	10	11	42		10	27	84
	11	9	29		11	25	71
	12	14	38		12	30	79
	13	13	25		13	29	67
	14	15	37		14	31	80
	15	12	24		15	28	66
U4	00	35	186	U5	00	51	229
	01	33	173		01	49	215
	02	34	187		02	50	228
	03	32	174		03	48	216
	04	39	182		04	55	225
	05	37	169		05	53	212
	06	38	183		06	54	224
	07	36	170		07	52	211
	08	42	207		08	58	249
	09	40	195		09	56	237
	10	43	208		10	59	250
	11	41	194		11	57	236
	12	46	203		12	62	245
	13	45	190		13	61	233
	14	47	204		14	63	246
	15	44	191		15	60	232

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

General Description

High-speed DDR4 SDRAM modules use DDR4 SDRAM devices with two or four internal memory bank groups. DDR4 SDRAM modules utilizing 4- and 8-bit-wide DDR4 SDRAM devices have four internal bank groups consisting of four memory banks each, providing a total of 16 banks. 16-bit-wide DDR4 SDRAM devices have two internal bank groups consisting of four memory banks each, providing a total of eight banks. DDR4 SDRAM modules benefit from DDR4 SDRAM's use of an $8n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR4 SDRAM effectively consists of a single $8n$ -bit-wide, four-clock data transfer at the internal DRAM core and eight corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR4 modules use two sets of differential signals: DQS_t and DQS_c to capture data and CK_t and CK_c to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR4 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR4.

Module Manufacturing Location

Micron Technology manufactures modules at sites world-wide. Customers may receive modules from any of the following manufacturing locations:

Table 7: DRAM Module Manufacturing Locations

Manufacturing Site Location	Country of Origin Specified on Label
Boise, USA	USA
Aguadilla, Puerto Rico	Puerto Rico
Xian, China	China
Singapore	Singapore

Address Mapping to DRAM

Address Mirroring

To achieve optimum routing of the address bus on DDR4 multi rank modules, the address bus will be wired as shown in the table below, or mirrored. For quad rank modules, ranks 1 and 3 are mirrored and ranks 0 and 2 are non-mirrored. Highlighted address pins have no secondary functions allowing for normal operation when cross-wired. Data is still read from the same address it was written. However, Load Mode operations require a specific address. This requires the controller to accommodate for a rank that is "mirrored." Systems may reference DDR4 SPD to determine if the module has mirroring implemented or not. See the JEDEC DDR4 SPD specification for more details.

Table 8: Address Mirroring

Edge Connector Pin	DRAM Pin, Non-mirrored	DRAM Pin, Mirrored
A0	A0	A0
A1	A1	A1
A2	A2	A2
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8
A8	A8	A7
A9	A9	A9
A10	A10	A10
A11	A11	A13
A13	A13	A11
A12	A12	A12
A14	A14	A14
A15	A15	A15
A16	A16	A16
A17	A17	A17
BA0	BA0	BA1
BA1	BA1	BA0
BG0	BG0	BG1
BG1	BG1	BG0

SPD EEPROM Operation

DDR4 SDRAM modules incorporate serial presence detect (SPD). The SPD data is stored in a 512-byte JEDEC JC-42.4-compliant EEPROM that is segregated into four 128-byte, write-protectable blocks. The SPD content is aligned with these blocks as shown in the table below.

Block	Range		Description
0	0–127	000h–07Fh	Configuration and DRAM parameters
1	128–255	080h–0FFh	Module-specific parameters
2	256–319	100h–13Fh	Reserved; all bytes coded as 00h
	320–383	140h–17Fh	Manufacturing information
3	384–511	180h–1FFh	End-user programmable

The first 384 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR4 SDRAM Modules." The remaining 128 bytes of storage are available for use by the customer.

The EEPROM resides on a two-wire I²C serial interface and is not integrated with the memory bus in any way. It operates as a slave device in the I²C bus protocol, with all operations synchronized by the serial clock. Transfer rates of up to 1 MHz are achievable at 2.5V (NOM).

Micron implements reversible software write protection on DDR4 SDRAM-based modules. This prevents the lower 384 bytes (bytes 0–383) from being inadvertently programmed or corrupted. The upper 128 bytes remain available for customer use and unprotected.

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 9: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	V_{DD} supply voltage relative to V_{SS}	-0.4	1.5	V	1
V_{DDQ}	V_{DDQ} supply voltage relative to V_{SS}	-0.4	1.5	V	1
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	-0.4	3.0	V	2
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4	1.5	V	

Table 10: Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage	1.14	1.2	1.26	V	1
V_{PP}	DRAM activating power supply	2.375	2.5	2.75	V	2
$V_{REFCA(DC)}$	Input reference voltage command/address bus	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V	3
I_{VTT}	Termination reference current from V_{TT}	-750	-	750	mA	
V_{TT}	Termination reference voltage (DC) – command/address bus	$0.49 \times V_{DD} - 20\text{mV}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD} + 20\text{mV}$	V	4
I_I	Input leakage current; any input excluding ZQ; $0V < V_{IN} < 1.1V$	-2.0	-	2.0	μA	5
$I_{I/O}$	DQ leakage; $0V < V_{in} < V_{DD}$	-4.0	-	4.0	μA	5
I_I	Input leakage current; ZQ	-3.0	-	3.0	μA	5, 6
I_{OZpd}	Output leakage current; $V_{OUT} = V_{DD}$; DQ is disabled	-	-	5.0	μA	
I_{OZpu}	Output leakage current; $V_{OUT} = V_{SS}$; DQ and ODT are disabled; ODT is disabled with ODT input HIGH	-	-	5.0	μA	
I_{VREFCA}	V_{REFCA} leakage; $V_{REFCA} = V_{DD}/2$ (after DRAM is initialized)	-2.0	-	2.0	μA	5

- Notes:
1. V_{DDQ} tracks with V_{DD} ; V_{DDQ} and V_{DD} are tied together.
 2. V_{PP} must be greater than or equal to V_{DD} at all times.
 3. V_{REFCA} must not be greater than $0.6 \times V_{DD}$. When V_{DD} is less than 500mV, V_{REF} may be less than or equal to 300mV.
 4. V_{TT} termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.
 5. Multiply by the number of DRAM die on the module.
 6. Tied to ground. Not connected to edge connector.

Table 11: Thermal Characteristics

Symbol	Parameter/Condition	Value	Units	Notes
T_C	Commercial operating case temperature	0 to 85	°C	1, 2, 3
T_C		>85 to 95	°C	1, 2, 3, 4
T_{OPER}	Normal operating temperature range	0 to 85	°C	5, 7
T_{OPER}	Extended temperature operating range (optional)	>85 to 95	°C	5, 7
T_{STG}	Non-operating storage temperature	-55 to 100	°C	6
RH_{STG}	Non-operating Storage Relative Humidity (non-condensing)	5 to 95	%	
NA	Change Rate of Storage Temperature	20	°C/hour	

- Notes:
1. Maximum operating case temperature; T_C is measured in the center of the package.
 2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T_C during operation.
 3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.
 4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 3.9µs interval refresh rate.
 5. The refresh rate must double when 85°C < T_{OPER} ≤ 95°C.
 6. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.
 7. For additional information, refer to technical note TN-00-08: "Thermal Applications" available at micron.com.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR4 component data sheets. Component specifications are available at micron.com. Module speed grades correlate with component speed grades, as shown below.

Table 12: Module and Component Speed Grades

DDR4 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-2G6	-075
-2G4	-083E
-2G3	-083
-2G1	-093E
-1G9	-107E

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the edge connector of the module, not at the DRAM. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

I_{DD} Specifications

Table 13: DDR4 I_{DD} Specifications and Conditions – 4GB (Die Revision B)

Values are for the MT40A512M16 DDR4 SDRAM only and are computed from values specified in the 8Gb (512 Meg x 16) component data sheet

Parameter	Symbol	2666	2400	2133	Units
One bank ACTIVATE-PRECHARGE current	I _{DD0}	340	320	300	mA
One bank ACTIVATE-PRECHARGE, Word Line Boost, I _{pp} current	I _{pp0}	16	16	16	mA
One bank ACTIVATE-READ-PRECHARGE current	I _{DD1}	420	400	380	mA
Precharge standby current	I _{DD2N}	252	244	236	mA
Precharge standby ODT current	I _{DD2NT}	300	300	268	mA
Precharge power-down current	I _{DD2P}	180	180	180	mA
Precharge quiet standby current	I _{DD2Q}	236	236	236	mA
Active standby current	I _{DD3N}	320	296	272	mA
Active standby I _{pp} current	I _{pp3N}	12	12	12	mA
Active power-down current	I _{DD3P}	252	236	220	mA
Burst read current	I _{DD4R}	916	836	756	mA
Burst write current	I _{DD4W}	876	796	716	mA
Burst refresh current (1x REF)	I _{DD5B}	1088	1088	1088	mA
Burst refresh I _{pp} current (1x REF)	I _{pp5B}	112	112	112	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I _{DD6N}	120	120	120	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I _{DD6E}	140	140	140	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I _{DD6R}	80	80	80	mA
Auto self refresh current (25°C)	I _{DD6A}	32	32	32	mA
Auto self refresh current (45°C)	I _{DD6A}	80	80	80	mA
Auto self refresh current (75°C)	I _{DD6A}	120	120	120	mA
Bank interleave read current	I _{DD7}	1036	996	956	mA
Bank interleave read I _{pp} current	I _{pp7}	60	60	60	mA
Maximum power-down current	I _{DD8}	100	100	100	mA

SPD EEPROM Operating Conditions

For the latest SPD data, refer to Micron's SPD page: micron.com/spd.

Table 14: SPD EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Nom	Max	Units
Supply voltage	V_{DDSPD}	–	2.5	–	V
Input low voltage: logic 0; all inputs	V_{IL}	–0.5	–	$V_{DDSPD} \times 0.3$	V
Input high voltage: logic 1; all inputs	V_{IH}	$V_{DDSPD} \times 0.7$	–	$V_{DDSPD} + 0.5$	V
Output low voltage: 3mA sink current $V_{DDSPD} > 2V$	V_{OL}	–	–	0.4	V
Input leakage current: (SCL, SDA) $V_{IN} = V_{DDSPD}$ or V_{SSSPD}	I_{LI}	–	–	±5	μA
Output leakage current: $V_{OUT} = V_{DDSPD}$ or V_{SSSPD} , SDA in High-Z	I_{LO}	–	–	±5	μA

- Notes: 1. Table is provided as a general reference. Consult JEDEC JC-42.4 EE1004 and TSE2004 device specifications for complete details.
2. All voltages referenced to V_{DDSPD} .

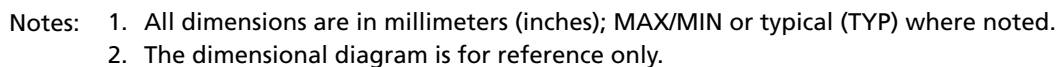
Table 15: SPD EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Clock frequency	t_{SCL}	10	1000	kHz
Clock pulse width HIGH time	t_{HIGH}	260	–	ns
Clock pulse width LOW time	t_{LOW}	500	–	ns
Detect clock LOW timeout	$t_{TIMEOUT}$	25	35	ms
SDA rise time	t_R	–	120	ns
SDA fall time	t_F	–	120	ns
Data-in setup time	$t_{SU:DAT}$	50	–	ns
Data-in hold time	$t_{HD:DI}$	0	–	ns
Data out hold time	$t_{HD:DAT}$	0	350	ns
Start condition setup time	$t_{SU:STA}$	260	–	ns
Start condition hold time	$t_{HD:STA}$	260	–	ns
Stop condition setup time	$t_{SU:STO}$	260	–	ns
Time the bus must be free before a new transition can start	t_{BUF}	500	–	ns
Write time	t_W	–	5	ms
Warm power cycle time off	t_{POFF}	1	–	ms
Time from power on to first command	t_{INIT}	10	–	ms

- Note: 1. Table is provided as a general reference. Consult JEDEC JC-42.4 EE1004 and TSE2004 device specifications for complete details.

Figure 3: 260-Pin DDR4 SODIMM

Figure 3: 260-Pin DDR4 SODIMM



This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.