



DDR3(L) 4GB / 8GB UDIMM

Features

- **JEDEC DDR3(L) Compliant¹**
 - 8n Prefetch Architecture
 - Differential Clock(CK/CK̅) and Data Strobe(DQS/DQS̅)
 - Double-data rate on DQs, DQS and DM
- **Data Integrity**
 - Auto Self Refresh (ASR) by DRAM built-in TS
 - Auto Refresh and Self Refresh Modes
- **Power Saving Mode**
 - Partial Array Self Refresh (PASR)²
 - Power Down Mode
- **Signal Integrity**
 - Configurable DS for system compatibility
 - Configurable On-Die Termination
 - ZQ Calibration
- **Signal Synchronization**
 - Write Leveling via MR settings³
 - Read Leveling via MPR
- **Residual Information**
 - Serial Presence-Detect (SPD) EEPROM
 - Fly-by I/O topology
 - Terminated control, command, and address bus

Options

- **Module / DRAM Speed Grade (CL-TRCD-TRP)⁴**
 - PC3(L)-12800 / DDR3(L)-1600 (11-11-11)
 - PC3(L)-12800 / DDR3(L)-1600 (9-9-9)
- **Temperature Range (T_A)**
 - 0°C ~ 65°C
- **Interface and Power Supply⁵**
 - DDR3(SSTL_15): VDD/VDDQ=1.5V(±0.075V)
 - DDR3L(SSTL_135): VDD/VDDQ=1.35V(-0.067/+0.1V)

Programmable Functions

- CAS Latency (5/6/7/8/9/10/11/12/13/14)
- CAS Write Latency (5/6/7/8/9/10)
- Additive Latency (0/CL-1/CL-2)
- Write Recovery Time (5/6/7/8/10/12/14/16)
- Burst Type (Sequential/Interleaved)
- Burst Length (BL8/BC4/BC4 or 8 on the fly)
- Self Refresh Temperature Range(Normal/Extended)
- Output Driver Impedance (34/40)
- On-Die Termination of Rtt_Nom(20/30/40/60/120)
- On-Die Termination of Rtt_WR(60/120)
- Precharge Power Down (slow/fast)

Packages / Density Information

Lead-free RoHS compliance and Halogen-free

Configuration	Pin count	PCB height (mm)	Mechanical Specifications
4GB (512Mbx64)	240	30	MO-269 R/C B
8GB (1024Mbx64)		30	MO-269 R/C B

Density and Addressing

DIMM	4GB	8GB
Rank Address	S0	2 (S[1:0])
DRAM Number	8	16
DRAM (512Mb x 8)	Refresh Count	8K
	Bank Address	8 (BA[2:0])
	Row Address	64K (A[15:0])
	Column Address	1K (A[9:0])
	tREFI ⁶	7.8μs
	tRFC ⁶	260ns

Notes:

- Based on NTC DDR3 4Gb C-Die component.
- Default state of PASR is disabled. This is enabled by using an electrical fuse. Please contact with NTC for the demand.
- Only Support prime DQ's feedback for each byte lane.
- The timing specification of high speed bin is backward compatible with low speed bin.
- SSTL_135 compatible to SSTL_15.
- Can not violate tREFI or tRFC.

DDR3(L) 4GB/8GB UDIMM

M2F(X)4G64CB88C4(5/7/H)N

M2F(X)8G64CB8HC4(5/9)N



Fundamental AC Specifications

DDR3(L)-1600 and DDR3(L)-1333

Speed Bins	DDR3(L)-1600		DDR3(L)-1333				Unit
	11-11-11		9-9-9		10-10-10		
Parameter	Min	Max	Min	Max	Min	Max	
tAA	13.75	20	13.5	20	15	20	ns
tRCD	13.75	-	13.5	-	15	-	ns
tRP	13.75	-	13.5	-	15	-	ns
tRC	48.75	-	49.5	-	51	-	ns
tRAS	35	9xtREFI	36	9xtREFI	36	9xtREFI	ns

DDR3(L)-1066 and DDR3(L)-800

Speed Bins	DDR3(L)-1066				DDR3(L)-800				Unit
	7-7-7		8-8-8		5-5-5		6-6-6		
Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
tAA	13.125	20	15	20	12.5	20	15	20	ns
tRCD	13.125	-	15	-	12.5	-	15	-	ns
tRP	13.125	-	15	-	12.5	-	15	-	ns
tRC	50.625	-	52.5	-	50	-	52.5	-	ns
tRAS	37.5	9xtREFI	37.5	9xtREFI	37.5	9xtREFI	37.5	9xtREFI	ns

Descriptions

M2F(X)4G64CB88C4(5/7/H)N / M2F(X)8G64CB8HC4(5/9)N are 240-Pin Double Data Rate 3 (DDR3) Synchronous DRAM Unbuffered Dual In-Line Memory Module (UDIMM), organized as one rank of 512Mx64 (4GB) and two ranks of 1024Mx64 (8GB) high-speed memory array. Modules use eight 512Mx8 (4GB) and sixteen 512Mx8 (8GB) 78-ball BGA packaged devices. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers.

The DIMM is intended for use in applications operating of 800MHz clock speeds and achieves high-speed data transfer rates of 12800Mbps. Prior to any access operation, the device $\overline{\text{CAS}}$ latency and burst/length/operation type must be programmed into the DIMM by address inputs and I/O inputs using the mode register set cycle. The DIMM uses serial presence-detect implemented via a serial EEPROM using a standard IIC protocol. The first 128 bytes of SPD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

DDR3(L) 4GB/8GB UDIMM

M2F(X)4G64CB88C4(5/7/H)N

M2F(X)8G64CB8HC4(5/9)N



Ordering Information

Organization	Part Number ¹	Heat Sink	Speed ²			
			Clock (MHz)	DIMM (Mbps)	DRAM (Mbps)	CL-TRCD-TRP
DDR3 (SSTL_15)						
512Mb x 64 (4GB)	M2X4G64CB88C4N-DG	NO	800	PC3-12800	DDR3-1600	9-9-9
	M2X4G64CB88C5N-DG	NO	800	PC3-12800	DDR3-1600	9-9-9
	M2X4G64CB88C7N-DG	NO	800	PC3-12800	DDR3-1600	9-9-9
	M2X4G64CB88CHN-DG	YES	800	PC3-12800	DDR3-1600	9-9-9
	M2F4G64CB88C4N-DI	NO	800	PC3-12800	DDR3-1600	11-11-11
	M2F4G64CB88C5N-DI	NO	800	PC3-12800	DDR3-1600	11-11-11
	M2F4G64CB88C7N-DI	NO	800	PC3-12800	DDR3-1600	11-11-11
1024Mb x 64 (8GB)	M2X8G64CB8HC4N-DG	NO	800	PC3-12800	DDR3-1600	9-9-9
	M2X8G64CB8HC5N-DG	NO	800	PC3-12800	DDR3-1600	9-9-9
	M2X8G64CB8HC9N-DG	YES	800	PC3-12800	DDR3-1600	9-9-9
	M2F8G64CB8HC4N-DI	NO	800	PC3-12800	DDR3-1600	11-11-11
	M2F8G64CB8HC5N-DI	NO	800	PC3-12800	DDR3-1600	11-11-11
	M2F8G64CB8HC9N-DI	YES	800	PC3-12800	DDR3-1600	11-11-11

NOTE 1 Bit 13 of part number stands for the combination of PCB version with/without heat sink.

NOTE 2 The timing specification of high speed bin is backward compatible with low speed bin.

DDR3(L) 4GB/8GB UDIMM

M2F(X)4G64CB88C4(5/7/H)N

M2F(X)8G64CB8HC4(5/9)N



Pin Description

Pin Name	Description	Pin Name	Description
CK[1:0]	Clock Inputs, positive line	SA[2:0]	Serial Presence Detect Address Inputs
$\overline{CK}$ [1:0]	Clock Inputs, negative line	DQ[63:0]	Data input/output
CKE[1:0]	Clock Enable	DQS[7:0]	Data strobes
$\overline{RAS}$	Row Address Strobe	$\overline{DQS}$ [7:0]	Data strobes complement
$\overline{CAS}$	Column Address Strobe	DM[7:0]	Data Masks
$\overline{WE}$	Write Enable	$\overline{RESET}$	Reset pin
$\overline{S}$ [1:0]	Chip Selects	V_{DD}, V_{DDQ}	Core and I/O power
A[9:0], A11, A[15:13]	Address Inputs	V_{SS}	Ground
A10/AP	Address Input/Auto-Precharge	V_{REFCA}, V_{REFDQ}	Input/output Reference
A12/ $\overline{BC}$	Address Input/Burst Chop	V_{DDSPD}	SPD power
BA[2:0]	SDRAM Bank Address Inputs	V_{TT}	Termination voltage
ODT[1:0]	Active termination control lines	NC	No Connect
SCL	Serial Presence Detect Clock Input		
SDA	Serial Presence Detect Data Input/Output		

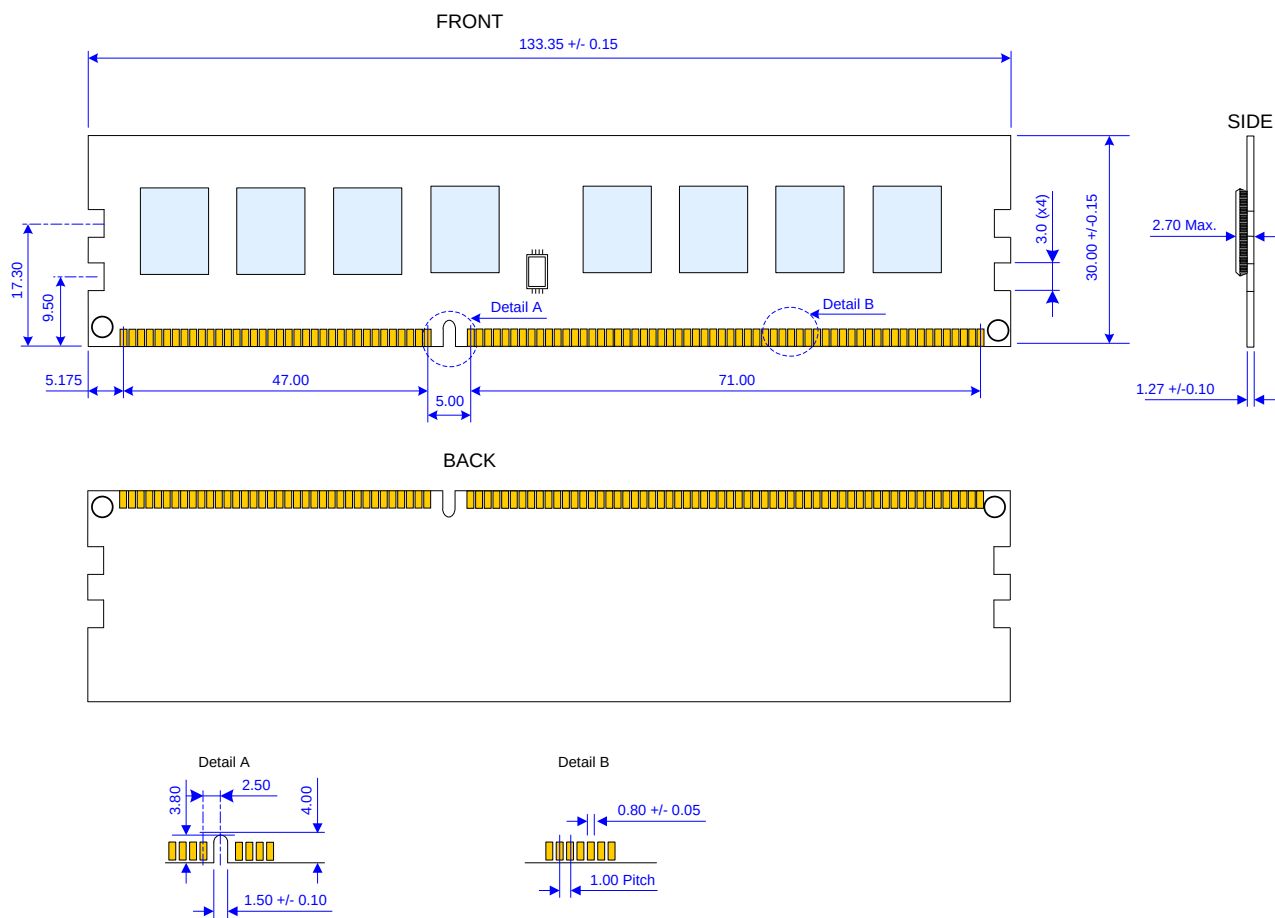
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4GB(1-Rank) Package Dimensions



Units: Millimeters

M2F(X)4G64CB88C4(5/7/H)N
M2F(X)8G64CB8HC4(5/9)N



DDR3(L) 4GB/8GB UDIMM

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Pin Assignment

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREFDQ	121	VSS	31	DQ25	151	VSS	61	A2	181	A1	91	DQ41	211	VSS
2	VSS	122	DQ4	32	VSS	152	DM3	62	VDD	182	VDD	92	VSS	212	DM5
3	DQ0	123	DQ5	33	$\overline{\text{DQS}}3$	153	NC	63	CK1,NC	183	VDD	93	$\overline{\text{DQS}}5$	213	NC
4	DQ1	124	VSS	34	DQS3	154	VSS	64	$\overline{\text{CK}}1, \text{NC}$	184	CK0	94	DQS5	214	VSS
5	VSS	125	DM0	35	VSS	155	DQ30	65	VDD	185	$\overline{\text{CK}}0$	95	VSS	215	DQ46
6	$\overline{\text{DQS}}0$	126	NC	36	DQ26	156	DQ31	66	VDD	186	VDD	96	DQ42	216	DQ47
7	DQS0	127	VSS	37	DQ27	157	VSS	67	VREFCA	187	NC	97	DQ43	217	VSS
8	VSS	128	DQ6	38	VSS	158	NC	68	NC	188	A0	98	VSS	218	DQ52
9	DQ2	129	DQ7	39	NC	159	NC	69	VDD	189	VDD	99	DQ48	219	DQ53
10	DQ3	130	VSS	40	NC	160	VSS	70	A10/AP	190	BA1	100	DQ49	220	VSS
11	VSS	131	DQ12	41	VSS	161	NC	71	BA0	191	VDD	101	VSS	221	DM6
12	DQ8	132	DQ13	42	$\overline{\text{NC}}$	162	NC	72	VDD	192	$\overline{\text{RAS}}$	102	$\overline{\text{DQS}}6$	222	NC
13	DQ9	133	VSS	43	NC	163	VSS	73	$\overline{\text{WE}}$	193	$\overline{\text{S}}0$	103	DQS6	223	VSS
14	VSS	134	DM1	44	VSS	164	NC	74	$\overline{\text{CAS}}$	194	VDD	104	VSS	224	DQ54
15	$\overline{\text{DQS}}1$	135	NC	45	NC	165	NC	75	VDD	195	ODT0	105	DQ50	225	DQ55
16	DQS1	136	VSS	46	NC	166	VSS	76	$\overline{\text{S}}1, \text{NC}$	196	A13	106	DQ51	226	VSS
17	VSS	137	DQ14	47	VSS	167	NC	77	ODT1,NC	197	VDD	107	VSS	227	DQ60
18	DQ10	138	DQ15	48	NC	168	$\overline{\text{RESET}}$	78	VDD	198	NC	108	DQ56	228	DQ61
19	DQ11	139	VSS	49	NC	169	CKE1/NC	79	NC	199	VSS	109	DQ57	229	VSS
20	VSS	140	DQ20	50	CKE0	170	VDD	80	VSS	200	DQ36	110	VSS	230	DM7
21	DQ16	141	DQ21	51	VDD	171	A15	81	DQ32	201	DQ37	111	$\overline{\text{DQS}}7$	231	NC
22	DQ17	142	VSS	52	BA2	172	A14	82	DQ33	202	VSS	112	DQS7	232	VSS
23	VSS	143	DM2	53	NC	173	VDD	83	VSS	203	DM4	113	VSS	233	DQ62
24	$\overline{\text{DQS}}2$	144	NC	54	VDD	174	A12/ $\overline{\text{BC}}$	84	$\overline{\text{DQS}}4$	204	NC	114	DQ58	234	DQ63
25	DQS2	145	VSS	55	A11	175	A9	85	DQS4	205	VSS	115	DQ59	235	VSS
26	VSS	146	DQ22	56	A7	176	VDD	86	VSS	206	DQ38	116	VSS	236	VDDSPD
27	DQ18	147	DQ23	57	VDD	177	A8	87	DQ34	207	DQ39	117	SA0	237	SA1
28	DQ19	148	VSS	58	A5	178	A6	88	DQ35	208	VSS	118	SCL	238	SDA
29	VSS	149	DQ28	59	A4	179	VDD	89	VSS	209	DQ44	119	SA2	239	VSS
30	DQ24	150	DQ29	60	VDD	180	A3	90	DQ40	210	DQ45	120	VTT	240	VTT

NOTE 1 CK1, $\overline{\text{CK}}1$, $\overline{\text{S}}1$, CKE1 and ODT1 are not used for 4GB UDIMM.

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M2F(X)4G64CB88C4(5/7/H)N

M2F(X)8G64CB8HC4(5/9)N



Input/Output Functional Descriptions

Symbol	Type	Polarity	Function
CK0, CK1 $\overline{\text{CK0}}, \overline{\text{CK1}}$	Input	Cross point	CK and $\overline{\text{CK}}$ are differential clock inputs. All the DDR3 SDRAM addr/cntl inputs are sampled on the crossing of positive edge of CK and negative edge of $\overline{\text{CK}}$. Output (read) data is referenced to the crossing of CK and $\overline{\text{CK}}$ (Both directions of crossing).
CKE[1:0]	Input	Active High	Activates the DDR3 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{\text{S}}[1:0]$	Input	Active Low	Enables the associated DDR3 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue, Rank 0 is selected by $\overline{\text{S0}}$; Rank 1 is selected by $\overline{\text{S1}}$.
$\overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WE}}$	Input	Active Low	$\overline{\text{RAS}}, \overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{S}}$) define the command being entered.
ODT[1:0]	Input	Active High	Asserts on-die termination for DQ, DM, DQS, and $\overline{\text{DQS}}$ signals if enabled via the DDR3 SDRAM mode register.
BA[2:0]	Input	-	Selects which DDR3 SDRAM internal bank of eight is activated.
A[9:0] A10/AP A11 A12/ $\overline{\text{BC}}$ A[15:13]	Input	-	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA[3:0] defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[3:0] to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA[3:0] inputs. If AP is low, then BA[3:0] are used to define which bank to precharge. A12/ $\overline{\text{BC}}$ is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH, no burst chop; LOW, burst chopped).
DM[7:0]	Input	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
DQS[7:0] $\overline{\text{DQS}}[7:0]$	I/O	Cross point	Data strobe for input and output data. For raw cards using x16 organized DRAMs, Pins DQ0–DQ7 are associated with the LDQS and $\overline{\text{LDQS}}$ pins and Pins DQ8–DQ15 are associated with UDQS and $\overline{\text{UDQS}}$ pins.
DQ[63:0]	I/O	-	Data Input/Output pins.
$V_{\text{DD}}, V_{\text{SS}}$	Supply	-	Power and ground for the DDR3 SDRAM input buffers, and core logic. VDD and VDDQ pins are tied to VDD/VDDQ planes on these modules.
V_{DDQ}	Supply	-	Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity. For all current DDR3 unbuffered DIMM designs, VDDQ shares the same power plane as VDD pins.
V_{DDSPD}	Supply	-	Power supply for SPD EEPROM. This supply is separate from the VDD/VDDQ power plane. EEPROM supply is operable from 3.0V to 3.6V.
$V_{\text{REFDQ}}, V_{\text{REFCA}}$	Supply	-	Reference voltage for inputs.
SDA	I/O	-	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pull up.
SCL	Input	-	This pin is used to clock data into and out of the SPD EEPROM. A resistor must be connected from the SCL bus line to V_{DDSPD} on the system planar to act as a pull up.
SA[2:0]	Input	-	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
$\overline{\text{RESET}}$	Input	-	The $\overline{\text{RESET}}$ pin is connected to the $\overline{\text{RESET}}$ pin on each DRAM. When low, all DRAMs are set to known state.
ZQ	Supply	-	Reference pin for ZQ calibration.

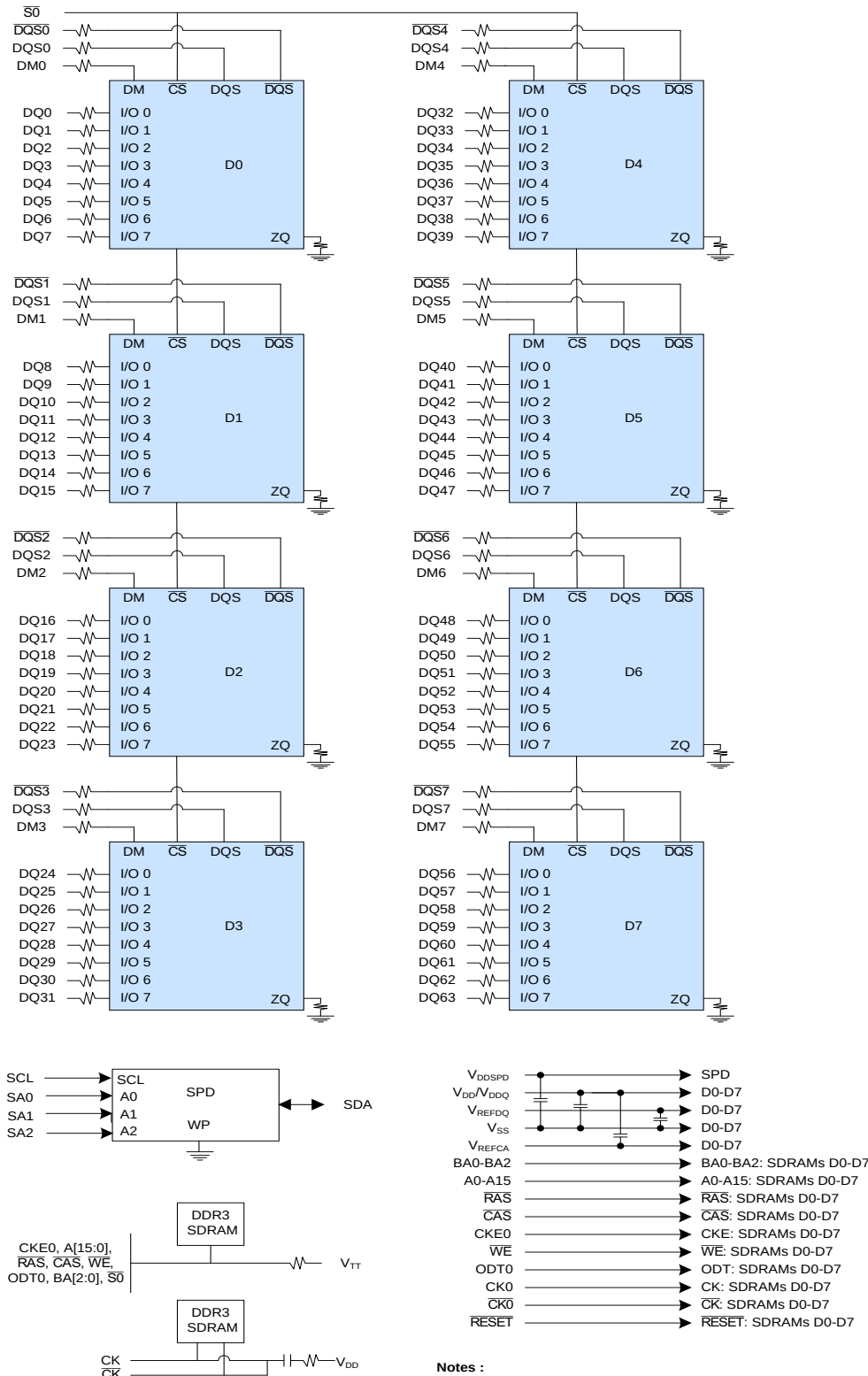
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M2F(X)8G64CB8HC4(5/9)N



4GB (1-Rank) Functional Block Diagram



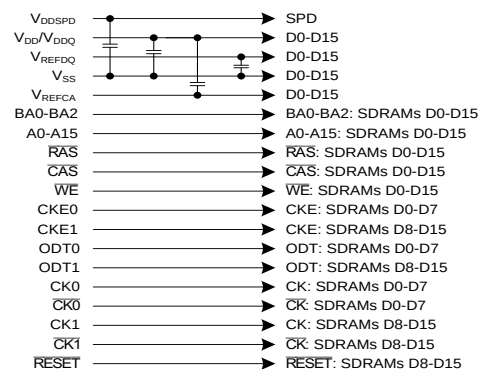
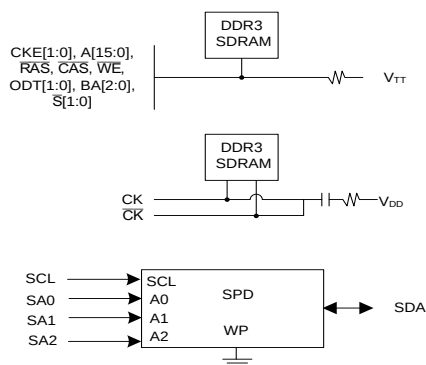
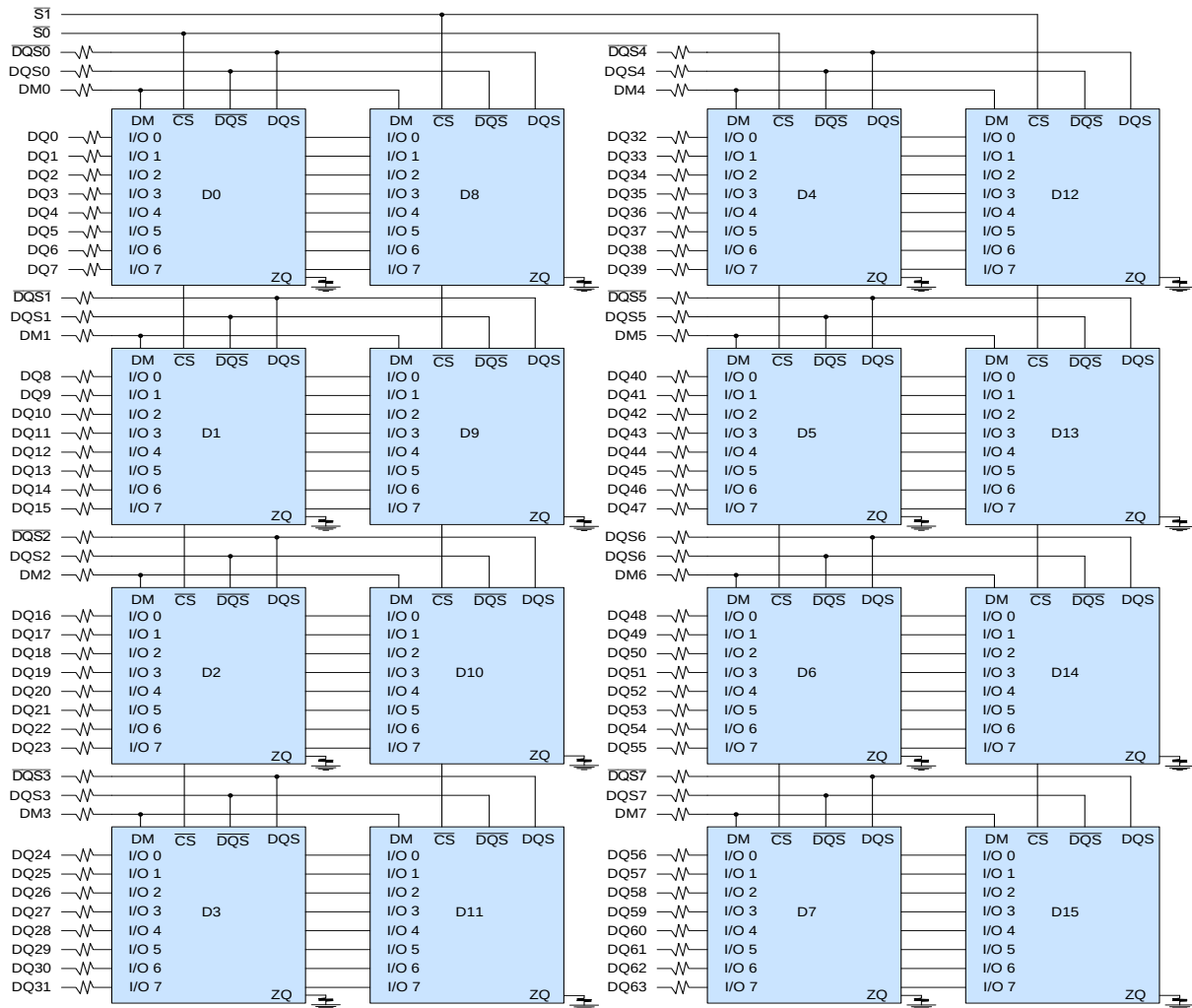
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8GB (2-Ranks) Functional Block Diagram



Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS#/ODT/DM/CKE/S relationships must be maintained as shown.
3. For each DRAM, a unique ZQ resistor is connected to ground. The ZQ resistor is 240Ω ±1%.
4. One SPD exists per module.

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M2F(X)8G64CB8HC4(5/9)N



DDR3L Operating, Standby, and Refresh Currents

Symbol	Parameter/Condition	4GB	8GB	Unit
IDD0	Operating One Bank Active-Precharge Current	282	414	mA
IDD1	Operating One Bank Active-Read-Precharge Current	367	500	mA
IDD2P0	Precharge Power-Down Current Slow Exit	51	102	mA
IDD2P1	Precharge Power-Down Current Fast Exit	52	104	mA
IDD2Q	Precharge Quiet Standby Current	104	208	mA
IDD2N	Precharge Standby Current	133	266	mA
IDD3P	Active Power-Down Current	99	197	mA
IDD3N	Active Standby Current	187	319	mA
IDD4R	Operating Burst Read Current	790	923	mA
IDD4W	Operating Burst Write Current	651	784	mA
IDD5B	Burst Refresh Current	880	1013	mA
IDD6	Self Refresh Current: Normal Temperature Range	76	151	mA
IDD7	Operating Bank Interleave Read Current	1212	1345	mA

DDR3 Operating, Standby, and Refresh Currents

Symbol	Parameter/Condition	4GB	8GB	Unit
IDD0	Operating One Bank Active-Precharge Current	309	461	mA
IDD1	Operating One Bank Active-Read-Precharge Current	405	557	mA
IDD2P0	Precharge Power-Down Current Slow Exit	57	114	mA
IDD2P1	Precharge Power-Down Current Fast Exit	58	116	mA
IDD2Q	Precharge Quiet Standby Current	121	241	mA
IDD2N	Precharge Standby Current	152	304	mA
IDD3P	Active Power-Down Current	212	424	mA
IDD3N	Active Standby Current	106	259	mA
IDD4R	Operating Burst Read Current	863	1016	mA
IDD4W	Operating Burst Write Current	722	875	mA
IDD5B	Burst Refresh Current	919	1071	mA
IDD6	Self Refresh Current: Normal Temperature Range	80	160	mA
IDD7	Operating Bank Interleave Read Current	1289	1441	mA

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Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit	Note
T _{OPER}	Operating Temperature (ambient)	0 to 65	°C	3
T _{STG}	Storage Temperature	-50 to 100	°C	1
T _{STG}	Storage Temperature (Plastic)	-55 to 100	°C	1
H _{STG}	Storage Humidity (without condensation)	5 to 95	%	1
P _{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1, 2

Note:

- Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Up to 9850 ft.
- The component maximum case temperature shall not exceed the value specified in the component spec.

Recommended DC Operating Conditions

Symbol	Parameter		Rating			Unit	Note
			Min.	Typ.	Max.		
VDDSPD	Core Supply Voltage	—	3.0	3.3	3.6	V	
VDD	Supply Voltage	DDR3	1.425	1.5	1.575	V	1,2
		DDR3L	1.283	1.35	1.45		3,4,5,6
VDDQ	Supply Voltage for Output	DDR3	1.425	1.5	1.575	V	1,2
		DDR3L	1.283	1.35	1.45		3,4,5,6

Note:

- Under all conditions VDDQ must be less than or equal to VDD.
- VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
- Maximum DC value may not be greater than 1.425V. The DC value is the linear average of VDD/ VDDQ(t) over a very long period of time (e.g., 1 sec).
- If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
- Under these supply voltages, the device operates to this DDR3L specification.
- Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3L operation.
- VDD= VDDQ= 1.35V (1.283 – 1.45V)
Backward compatible to VDD= VDDQ= 1.5V $\pm 0.075V$
Supports DDR3L devices to be backward compatible in 1.5V applications

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Revision History

Version	Page	Modified	Description	Released
1.0	-	-	Official Release.	12/2013
1.1	-	-	1. Add Part Number to ordering info. 2. Add DDR3L Spec	12/2013
1.2	P4	-	Remove 1.35V part number.	02/2014



<http://www.elixir-memory.com/>