KVR13LR9S8L/2HC

2GB 1Rx8 256M x 72-Bit PC3L-10600
CL9 Registered w/Parity 240-Pin DIMM

DRAM Supported: Hynix C-Die

DESCRIPTION

This document describes ValueRAM's 256M x 72-bit (2GB) DDR3L-1333 CL9 SDRAM (Synchronous DRAM), low voltage, registered w/parity, 1Rx8, ECC, VLP (very low profile) memory module, based on nine 256M x 8-bit DDR3L-1333 FBGA components. The SPD is programmed to JEDEC standard latency DDR3-1333 timing of 9-9-9 at 1.35V and 1.5V. This 240-pin DIMM uses gold contact fingers. The electrical and mechanical specifications are as follows:

FEATURES

- JEDEC standard 1.35V (1.28V ~ 1.45V) and 1.5V (1.425V ~ 1.575V) Power Supply
- VDDQ = 1.35V (1.28V ~ 1.45V) and 1.5V (1.425V ~ 1.575V)
- 667MHz fCK for 1333Mb/sec/pin
- 8 independent internal bank
- Programmable CAS Latency: 9, 8, 7, 6
- Programmable Additive Latency: 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency(CWL) = 7 (DDR3-1333)
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address “000” only), 4 with tCCD = 4 which does not allow seamless read or write [either on the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)
- On Die Termination using ODT pin
- On-DIMM thermal sensor (Grade B)
- Average Refresh Period 7.8us at lower than TCASE 85°C, 3.9us at 85°C < TCASE ≤ 95°C
- Asynchronous Reset
- PCB : Height 0.740” (18.75mm), double sided component

SPECIFICATIONS

CL(IDD)	9 cycles
Row Cycle Time (tRCmin)	49.5ns (min.)
Refresh to Active/Refresh Command Time (tRFCmin)	160ns (min.)
Row Active Time (tRASmin)	36ns (min.)
Maximum Operating Power	(1.35V) = 3.036 W* (1.50V) = 3.576 W*
UL Rating	94 V - 0
Operating Temperature	0° C to 85° C
Storage Temperature	-55° C to +100° C

*Power will vary depending on the SDRAM and Register/PLL used.

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MODULE DIMENSIONS:



