

DDR5 SDRAM EUDIMM Addendum

MTC20C2085S1EC – 32GB 16Gb Die Revision A

Features

Information provided here is in addition to or supercedes information provided in the Micron DDR5 UDIMM Core data sheet.

- DDR5 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the Micron DDR5 UDIMM core data sheet
- 288-pin, DDR5 unbuffered ECC dual in-line memory module (DDR5 EUDIMM)
- Fast data transfer rate: PC5-4800
- 32GB (4Gig x 72)
- Dual-rank
- 32 internal banks; 8 groups of 4 banks each
- Supports ECC error detection and correction

Options

- Operating temperature
 - Commercial ($0^{\circ}\text{C} \leq T_{\text{OPER}} \leq 95^{\circ}\text{C}$)
- Frequency/CAS latency
 - 0.416ns @ CL = 40 (DDR5-4800)

Marking

C

48B

Figure 1: 288-Pin DDR5 EUDIMM (R/C-E0)

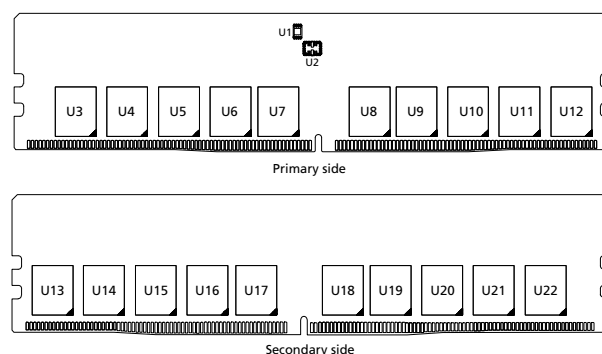


Table 1: Addressing

Parameter	32GB
Row address ¹	64K (R0-R15)
Column address ¹	1K (C0-C9)
Device bank group address ¹	8 (BG0-BG2)
Device bank address per bank group ¹	4 (BA0-BA1)
Device configuration	16Gb (2Gb x 8), 32 banks
Module rank address	2 (CS0_n, CS1_n)

Notes: 1. These parameters represent the logical address state of the CA bus for different commands. Refer to the command truth table in the component data sheet.

Table 2: Part Numbers and Timing Parameters – 32GB Modules

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-nRCD-nRP)
MTC20C2085S1EC48BA1	32GB	4Gb x 72	38.4 GB/s	0.416ns/4800 MT/s	40-39-39

Notes: 1. Base device: MT60B2G8, 16Gb DDR5 SDRAM Die Revision A. The data sheet for the base device can be found on [micron.com](https://www.micron.com).



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DQ Map

Table 3: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U3	0	3A	156	U4	0	11A	166
	1	2A	154		1	8A	20
	2	1A	11		2	10A	164
	3	0A	9		3	9A	22
	4	7A	162		4	15A	173
	5	4A	16		5	12A	26
	6	5A	18		6	13A	28
	7	6A	160		7	14A	171
U5	0	23A	183	U6	0	29A	49
	1	20A	37		1	28A	47
	2	22A	181		2	31A	194
	3	21A	39		3	30A	192
	4	19A	177		4	27A	187
	5	16A	30		5	24A	41
	6	18A	175		6	25A	43
	7	17A	32		7	26A	185
U7	0	CB3A	198	U8	0	CB1B	99
	1	CB0A	51		1	CB0B	97
	2	CB2A	196		2	CB3B	244
	3	CB1A	53		3	CB2B	242
	4	–	–		4	–	–
	5	–	–		5	–	–
	6	–	–		6	–	–
	7	–	–		7	–	–
U9	0	3B	248	U10	0	10B	256
	1	0B	101		1	8B	112
	2	2B	246		2	11B	258
	3	1B	103		3	9B	114
	4	7B	254		4	15B	265
	5	4B	108		5	12B	118
	6	5B	110		6	13B	120
	7	6B	252		7	14B	263



32GB (x72, DR) 288-Pin DDR5 ECC UDIMM DQ Map

Table 3: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U11	0	18B	267	U12	0	29B	141
	1	17B	124		1	28B	139
	2	19B	269		2	31B	286
	3	16B	122		3	30B	284
	4	23B	275		4	27B	279
	5	20B	129		5	24B	133
	6	21B	131		6	26B	277
	7	22B	273		7	25B	135
U13	0	28B	139	U14	0	17B	124
	1	29B	141		1	18B	267
	2	30B	284		2	16B	122
	3	31B	286		3	19B	269
	4	24B	133		4	20B	129
	5	27B	279		5	23B	275
	6	25B	135		6	22B	273
	7	26B	277		7	21B	131
U15	0	8B	112	U16	0	0B	101
	1	10B	256		1	3B	248
	2	9B	114		2	1B	103
	3	11B	258		3	2B	246
	4	12B	118		4	4B	108
	5	15B	265		5	7B	254
	6	14B	263		6	6B	252
	7	13B	120		7	5B	110
U17	0	CB0B	97	U18	0	CB0A	51
	1	CB1B	99		1	CB3A	198
	2	CB2B	242		2	CB1A	53
	3	CB3B	244		3	CB2A	196
	4	–	–		4	–	–
	5	–	–		5	–	–
	6	–	–		6	–	–
	7	–	–		7	–	–



Table 3: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U19	0	28A	47	U20	0	20A	37
	1	29A	49		1	23A	183
	2	30A	192		2	21A	39
	3	31A	194		3	22A	181
	4	24A	41		4	16A	30
	5	27A	187		5	19A	177
	6	26A	185		6	17A	32
	7	25A	43		7	18A	175
U21	0	8A	20	U22	0	2A	154
	1	11A	166		1	3A	156
	2	9A	22		2	0A	9
	3	10A	164		3	1A	11
	4	12A	26		4	4A	16
	5	15A	173		5	7A	162
	6	14A	171		6	6A	160
	7	13A	28		7	5A	18

I_{DD} Specifications

Table 4: DDR5 I_{DD} Specifications and Conditions – 32GB (Die Revision A)

Module I_{DD} is based on PMIC VIN_BULK 5V input current and typical operating range of temperature. Each I_{DD} parameter includes PMIC efficiency and all DRAM current on all supplies (V_{DD}, V_{DDQ}, and V_{PP}).

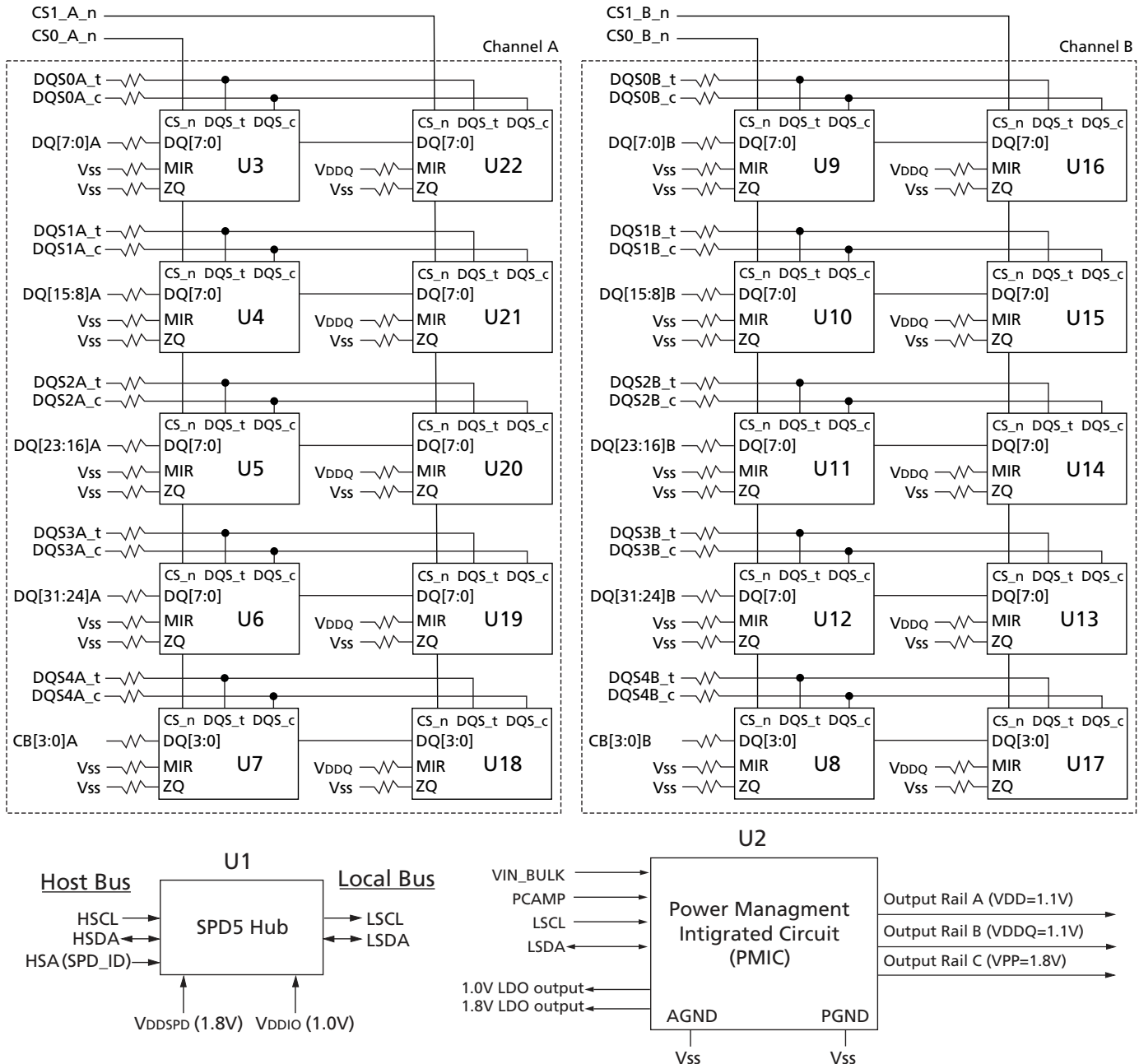
Parameter	Symbol	4800	Units
Operating one bank ACTIVATE-PRECHARGE current	I _{DD0} ¹	190	mA
Operating four bank ACTIVATE-PRECHARGE current	I _{DD0F} ¹	276	mA
Precharge standby current	I _{DD2N} ²	169	mA
Precharge standby non-target command	I _{DD2NT} ¹	229	mA
Precharge power-down current	I _{DD2P} ²	144	mA
Active standby current	I _{DD3N} ²	205	mA
Active power-down current	I _{DD3P} ²	180	mA
Operating burst read current	I _{DD4R} ¹	767	mA
Operating burst write current	I _{DD4W} ¹	1028	mA
Operating burst write with write CRC current	I _{DD4WC} ¹	936	mA
Burst refresh (normal refresh mode) current	I _{DD5B} ¹	563	mA
Burst refresh (fine granularity refresh mode) current	I _{DD5F} ¹	539	mA
Burst refresh (same bank refresh mode) current	I _{DD5C} ¹	276	mA
Self refresh current	I _{DD6N} ²	118	mA
Operating bank interleave read current	I _{DD7} ¹	1118	mA
Maximum power saving deep power down mode current	I _{DD8} ²	77	mA

Notes: 1. One module rank in this I_{DD}/I_{DDQ}/I_{PP} condition, the other rank in I_{DD2N}/I_{DDQ2N}/I_{PP2N}.

2. Both ranks in this I_{DD}/I_{DDQ}/I_{PP} condition.

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR5 component is connected to an external $240\Omega \pm 1\%$ resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.



Revision History

Rev. B – 12/2022

- Added MIR state to Functional Block Diagram
- Removed Micron Confidential designation

Rev. A – 01/2022

- Production Release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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