



DDR3(L) 4GB / 8GB SODIMM

Features

- **JEDEC DDR3(L) Compliant¹**
 - 8n Prefetch Architecture
 - Differential Clock(CK/CK $\bar{K}$) and Data Strobe(DQS/DQS $\bar{S}$)
 - Double-data rate on DQs, DQS and DM
- **Data Integrity**
 - Auto Self Refresh (ASR) by DRAM built-in TS
 - Auto Refresh and Self Refresh Modes
- **Power Saving Mode**
 - Partial Array Self Refresh (PASR)²
 - Power Down Mode
- **Signal Integrity**
 - Configurable DS for system compatibility
 - Configurable On-Die Termination
 - ZQ Calibration
- **Signal Synchronization**
 - Write Leveling via MR settings³
 - Read Leveling via MPR
- **Residual Information**
 - Serial Presence-Detect (SPD) EEPROM
 - Fly-by I/O topology
 - Terminated control, command, and address bus

Options

- **Module / DRAM Speed Grade (CL-TRCD-TRP)⁴**
 - PC3(L)-10600 / DDR3(L)-1333 (9-9-9)
 - PC3(L)-12800 / DDR3(L)-1600 (11-11-11)
- **Temperature Range (T_A)**
 - 0°C ~ 65°C
- **Interface and Power Supply⁵**
 - DDR3(SSTL_15): VDD/VDDQ=1.5V(±0.075V)
 - DDR3L(SSTL_135): VDD/VDDQ=1.35V(-0.067/+0.1V)

Programmable Functions

- **CAS Latency (5/6/7/8/9/10/11/12/13/14)**
- **CAS Write Latency (5/6/7/8/9/10)**
- **Additive Latency (0/CL-1/CL-2)**
- **Write Recovery Time (5/6/7/8/10/12/14/16)**
- **Burst Type (Sequential/Interleaved)**
- **Burst Length (BL8/BC4/BC4 or 8 on the fly)**
- **Self Refresh Temperature Range(Normal/Extended)**
- **Output Driver Impedance (34/40)**
- **On-Die Termination of Rtt_Nom(20/30/40/60/120)**
- **On-Die Termination of Rtt_WR(60/120)**
- **Precharge Power Down (slow/fast)**

Packages / Density Information

Lead-free RoHS compliance and Halogen-free

Configuration	Pin count	PCB height (mm)	Mechanical Specifications
4GB (512Mbx64)	204	30	MO-268 R/C B
8GB (1024Mbx64)		30	MO-268 R/C F

Density and Addressing

DIMM	4GB	8GB
Rank Address	S0	2 (S[1:0])
DRAM Number	8	16
Refresh Count	8K	
Bank Address	8 (BA[2:0])	
Row Address	64K (A[15:0])	
Column Address	1K (A[9:0])	
tREFI ⁶	7.8μs	
tRFC ⁶	260ns	

NOTE 1 Based on NTC DDR3 4Gb B-Die component.

NOTE 2 Default state of PASR is disabled. This is enabled by using an electrical fuse. Please contact with NTC for the demand.

NOTE 3 Only Support prime DQ's feedback for each byte lane.

NOTE 4 The timing specification of high speed bin is backward compatible with low speed bin.

NOTE 5 1.35V DDR3L are backward compatible to 1.5V DDR3 parts. 1.35V DDR3L-RS parts are exceptional and unallowable to be compatible to 1.35V DDR3L and 1.5V DDR3 parts

NOTE 6 Violating tRFC specification will induce malfunction. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9us interval refresh rate. Extended SRT or ASR must be enabled.

Fundamental AC Specifications

DDR3(L)-1600 and DDR3(L)-1333

Speed Bins	DDR3(L)-1600		DDR3(L)-1333				Unit
	11-11-11		9-9-9		10-10-10		
Parameter	Min	Max	Min	Max	Min	Max	
tAA	13.75	20	13.5	20	15	20	ns
tRCD	13.75	-	13.5	-	15	-	ns
tRP	13.75	-	13.5	-	15	-	ns
tRC	48.75	-	49.5	-	51	-	ns
tRAS	35	9xtREFI	36	9xtREFI	36	9xtREFI	ns

DDR3(L)-1066 and DDR3(L)-800

Speed Bins	DDR3(L)-1066				DDR3(L)-800				Unit
	7-7-7		8-8-8		5-5-5		6-6-6		
Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
tAA	13.125	20	15	20	12.5	20	15	20	ns
tRCD	13.125	-	15	-	12.5	-	15	-	ns
tRP	13.125	-	15	-	12.5	-	15	-	ns
tRC	50.625	-	52.5	-	50	-	52.5	-	ns
tRAS	37.5	9xtREFI	37.5	9xtREFI	37.5	9xtREFI	37.5	9xtREFI	ns

Descriptions

M2S4G64CB(C)88B4(5)N and M2S8G64CB(C)8HB4(5)N are unbuffered 204-Pin Double Data Rate 3 (DDR3) Synchronous DRAM Small Outline Dual In-Line Memory Module (SO-DIMM), organized as one rank of 512Mx64 (4GB) and two ranks of 1024Mx64 (8GB) high-speed memory array. Modules use eight 512Mx8 (4GB) and sixteen 512Mx8 (8GB) 78-ball BGA packaged devices. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers.

All Elixir DDR3 SODIMMs provide a high-performance, flexible 8-byte interface in a space-saving footprint. The DIMM is intended for use in applications operating of 667MHz/800MHz clock speeds and achieves high-speed data transfer rates of 10600Mbps/12800Mbps. Prior to any access operation, the device CAS latency and burst/length/operation type must be programmed into the DIMM by address inputs and I/O inputs using the mode register set cycle. The DIMM uses serial presence-detect implemented via a serial EEPROM using a standard IIC protocol. The first 128 bytes of SPD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

Ordering Information

Organization	Part Number ¹	Speed ²			
		Clock (MHz)	DIMM (Mbps)	DRAM (Mbps)	CL-TRCD-TRP
DDR3 (SSTL_15)					
512Mb x 64 (4GB)	M2S4G64CB88B4N-CG	667	PC3-10600	DDR3-1333	9-9-9
	M2S4G64CB88B5N-CG	667	PC3-10600	DDR3-1333	9-9-9
	M2S4G64CB88B4N-DI	800	PC3-12800	DDR3-1600	11-11-11
	M2S4G64CB88B5N-DI	800	PC3-12800	DDR3-1600	11-11-11
1024Mb x 64 (8GB)	M2S8G64CB8HB4N-CG	667	PC3-10600	DDR3-1333	9-9-9
	M2S8G64CB8HB5N-CG	667	PC3-10600	DDR3-1333	9-9-9
	M2S8G64CB8HB4N-DI	800	PC3-12800	DDR3-1600	11-11-11
	M2S8G64CB8HB5N-DI	800	PC3-12800	DDR3-1600	11-11-11
DDR3L (SSTL_135)					
512Mb x 64 (4GB)	M2S4G64CC88B4N-CG	667	PC3L-10600	DDR3-1333	9-9-9
	M2S4G64CC88B5N-CG	667	PC3L -10600	DDR3-1333	9-9-9
	M2S4G64CC88B4N-DI	800	PC3L-12800	DDR3-1600	11-11-11
	M2S4G64CC88B5N-DI	800	PC3L-12800	DDR3-1600	11-11-11
1024Mb x 64 (8GB)	M2S8G64CC8HB4N-CG	667	PC3L-10600	DDR3-1333	9-9-9
	M2S8G64CC8HB5N-CG	667	PC3L-10600	DDR3-1333	9-9-9
	M2S8G64CC8HB4N-DI	800	PC3L-12800	DDR3-1600	11-11-11
	M2S8G64CC8HB5N-DI	800	PC3L-12800	DDR3-1600	11-11-11

NOTE 1 Bit 13 of part number stands for PCB version.

NOTE 2 The timing specification of high speed bin is backward compatible with low speed bin.

DDR3(L) 4GB/8GB SODIMM

M2S4G64CB(C)88B4(5)N / M2S8G64CB(C)8HB4(5)N



Pin Description

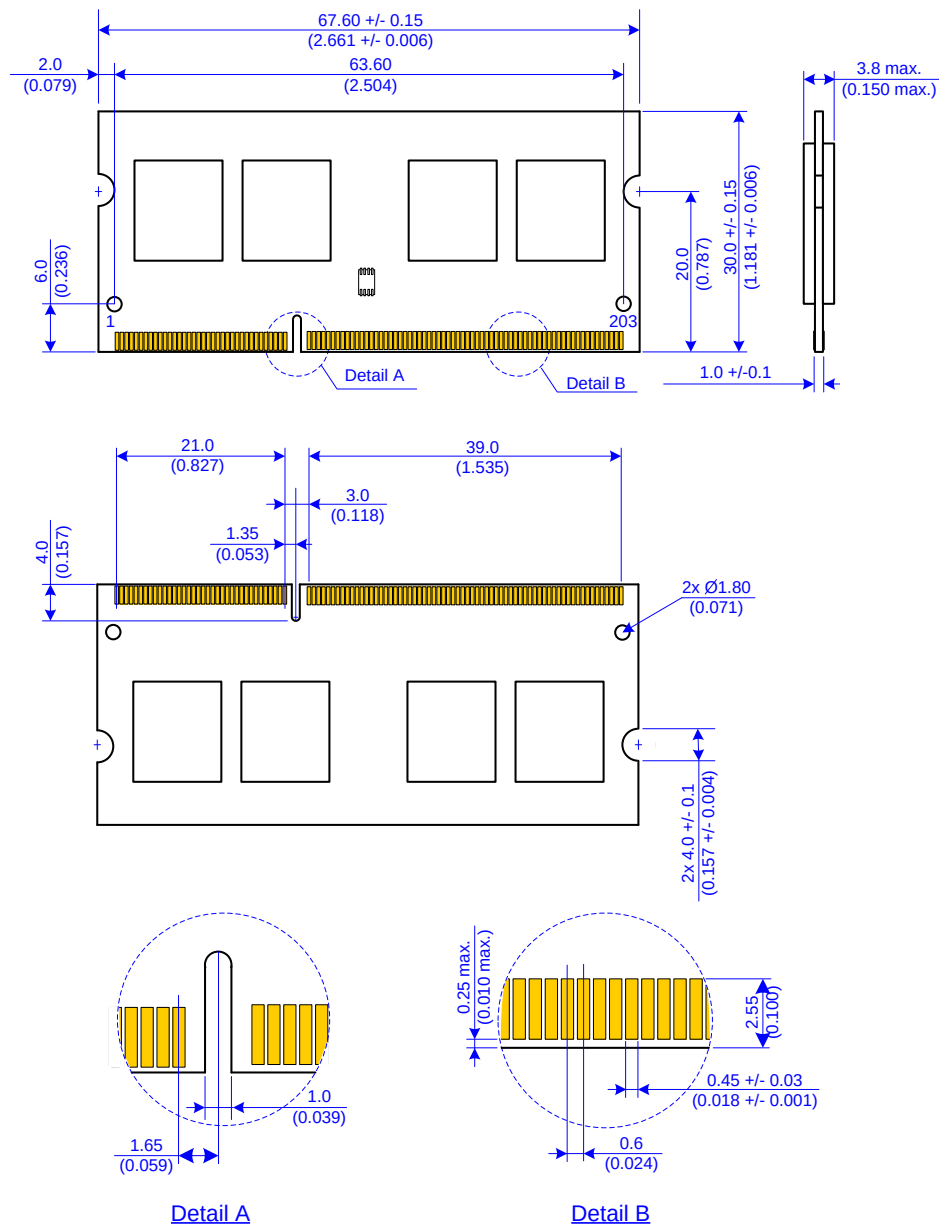
Pin Name	Description	Count	Pin Name	Description	Count
CK[1:0]	Clock Inputs, positive line	2	SA[1:0]	Serial Presence Detect Address Inputs	2
$\overline{\text{CK}}$ [1:0]	Clock Inputs, negative line	2	DQ[63:0]	Data input/output	64
CKE[1:0]	Clock Enable	2	DQS[7:0]	Data strobes	8
$\overline{\text{RAS}}$	Row Address Strobe	1	$\overline{\text{DQS}}$ [7:0]	Data strobes complement	8
$\overline{\text{CAS}}$	Column Address Strobe	1	DM[7:0]	Data Masks	8
$\overline{\text{WE}}$	Write Enable	1	$\overline{\text{RESET}}$	Reset pin	1
$\overline{\text{S}}$ [1:0]	Chip Selects	2	V _{DD}	Core and I/O power	18
A[9:0], A11, A[15:13]	Address Inputs	14	V _{SS}	Ground	52
A10/AP	Address Input/Auto-Precharge	1	V _{REFCA} , V _{REFDQ}	Input/output Reference	2
A12/ $\overline{\text{BC}}$	Address Input/Burst Chop	1	V _{DDSPD}	SPD power	1
BA[2:0]	SDRAM Bank Address Inputs	3	V _{TT}	Termination voltage	2
ODT[1:0]	Active termination control lines	2	NC	No Connect	4
SCL	Serial Presence Detect Clock Input	1			
SDA	Serial Presence Detect Data Input/Output	1			
				Total	204

DDR3(L) 4GB/8GB SODIMM

M2S4G64CB(C)88B4(5)N / M2S8G64CB(C)8HB4(5)N



4GB(1-Rank) Package Dimensions



Units: Millimeters (Inches)

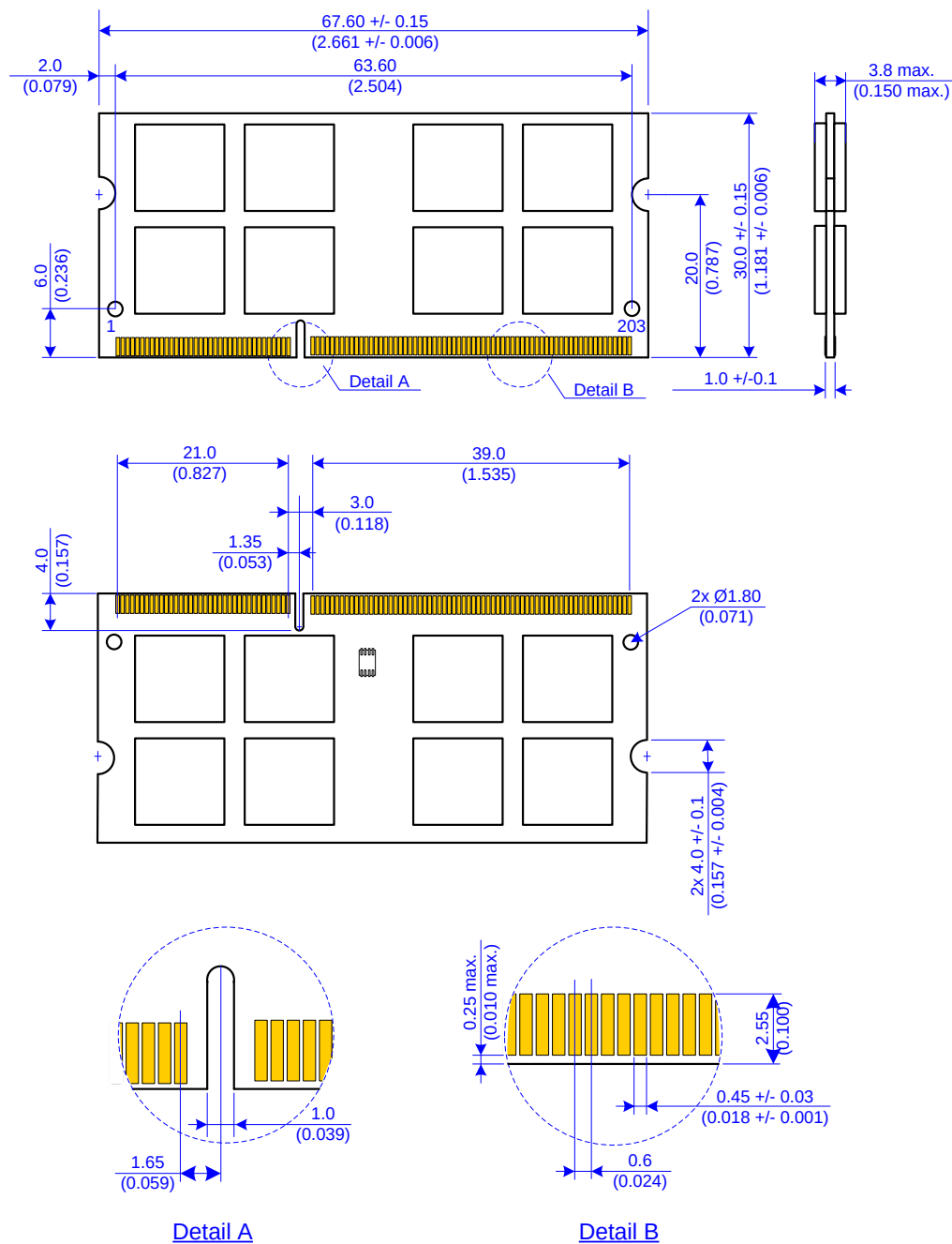
NOTE 1 Device position and scale are only for reference.

DDR3(L) 4GB/8GB SODIMM

M2S4G64CB(C)88B4(5)N / M2S8G64CB(C)8HB4(5)N



8GB(2-Ranks) Package Dimensions



Units: Millimeters (Inches)

NOTE 1 Device position and scale are only for reference.

DDR3(L) 4GB/8GB SODIMM

M2S4G64CB(C)88B4(5)N / M2S8G64CB(C)8HB4(5)N



Pin Assignment

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V _{REFDQ}	2	V _{SS}	53	DQ19	54	V _{SS}	105	V _{DD}	106	V _{DD}	155	V _{SS}	156	V _{SS}
3	V _{SS}	4	DQ4	55	V _{SS}	56	DQ28	107	A10/AP	108	BA1	157	DQ42	158	DQ46
5	DQ0	6	DQ5	57	DQ24	58	DQ29	109	BA0	110	RAS ⁻	159	DQ43	160	DQ47
7	DQ1	8	V _{SS}	59	DQ25	60	V _{SS}	111	V _{DD}	112	V _{DD}	161	V _{SS}	162	V _{SS}
9	V _{SS}	10	DQS0	61	V _{SS}	62	DQS3	113	WE	114	S0	163	DQ48	164	DQ52
11	DM0	12	DQS0	63	DM3	64	DQS3	115	CAS	116	ODT0	165	DQ49	166	DQ53
13	V _{SS}	14	V _{SS}	65	V _{SS}	66	V _{SS}	117	V _{DD}	118	V _{DD}	167	V _{SS}	168	V _{SS}
15	DQ2	16	DQ6	67	DQ26	68	DQ30	119	A13/NC	120	ODT1	169	DQS6	170	DM6
17	DQ3	18	DQ7	69	DQ27	70	DQ31	121	ST	122	NC	171	DQS6	172	V _{SS}
19	V _{SS}	20	V _{SS}	71	V _{SS}	72	V _{SS}	123	V _{DD}	124	V _{DD}	173	V _{SS}	174	DQ54
21	DQ8	22	DQ12	73	CKE0	74	CKE1	125	NC	126	V _{REFCA}	175	DQ50	176	DQ55
23	DQ9	24	DQ13	75	V _{DD}	76	V _{DD}	127	V _{SS}	128	V _{SS}	177	DQ51	178	V _{SS}
25	V _{SS}	26	V _{SS}	77	NC	78	A15	129	DQ32	130	DQ36	179	V _{SS}	180	DQ60
27	DQS1	28	DM1	79	BA2	80	A14	131	DQ33	132	DQ37	181	DQ56	182	DQ61
29	DQS1	30	RESET	81	V _{DD}	82	V _{DD}	133	V _{SS}	134	V _{SS}	183	DQ57	184	V _{SS}
31	V _{SS}	32	V _{SS}	83	A12/BC	84	A11	135	DQS4	136	DM4	185	V _{SS}	186	DQS7
33	DQ10	34	DQ14	85	A9	86	A7	137	DQS4	138	V _{SS}	187	DM7	188	DQS7
35	DQ11	36	DQ15	87	V _{DD}	88	V _{DD}	139	V _{SS}	140	DQ38	189	V _{SS}	190	V _{SS}
37	V _{SS}	38	V _{SS}	89	A8	90	A6	141	DQ34	142	DQ39	191	DQ58	192	DQ62
39	DQ16	40	DQ20	91	A5	92	A4	143	DQ35	144	V _{SS}	193	DQ59	194	DQ63
41	DQ17	42	DQ21	93	V _{DD}	94	V _{DD}	145	V _{SS}	146	DQ44	195	V _{SS}	196	V _{SS}
43	V _{SS}	44	V _{SS}	95	A3	96	A2	147	DQ40	148	DQ45	197	SA0	198	NC
45	DQS2	46	DM2	97	A1	98	A0	149	DQ41	150	V _{SS}	199	V _{DDSPD}	200	SDA
47	DQS2	48	V _{SS}	99	V _{DD}	100	V _{DD}	151	V _{SS}	152	DQS5	201	SA1	202	SCL
49	V _{SS}	50	DQ22	101	CK0	102	CK1	153	DM5	154	DQS5	203	V _{tt}	204	V _{tt}
51	DQ18	52	DQ23	103	CK0	104	CK1								

NOTE 1 CK1, CK1, S1, CKE1 and ODT1 are not used for 4GB SODIMM.

Input/Output Functional Descriptions

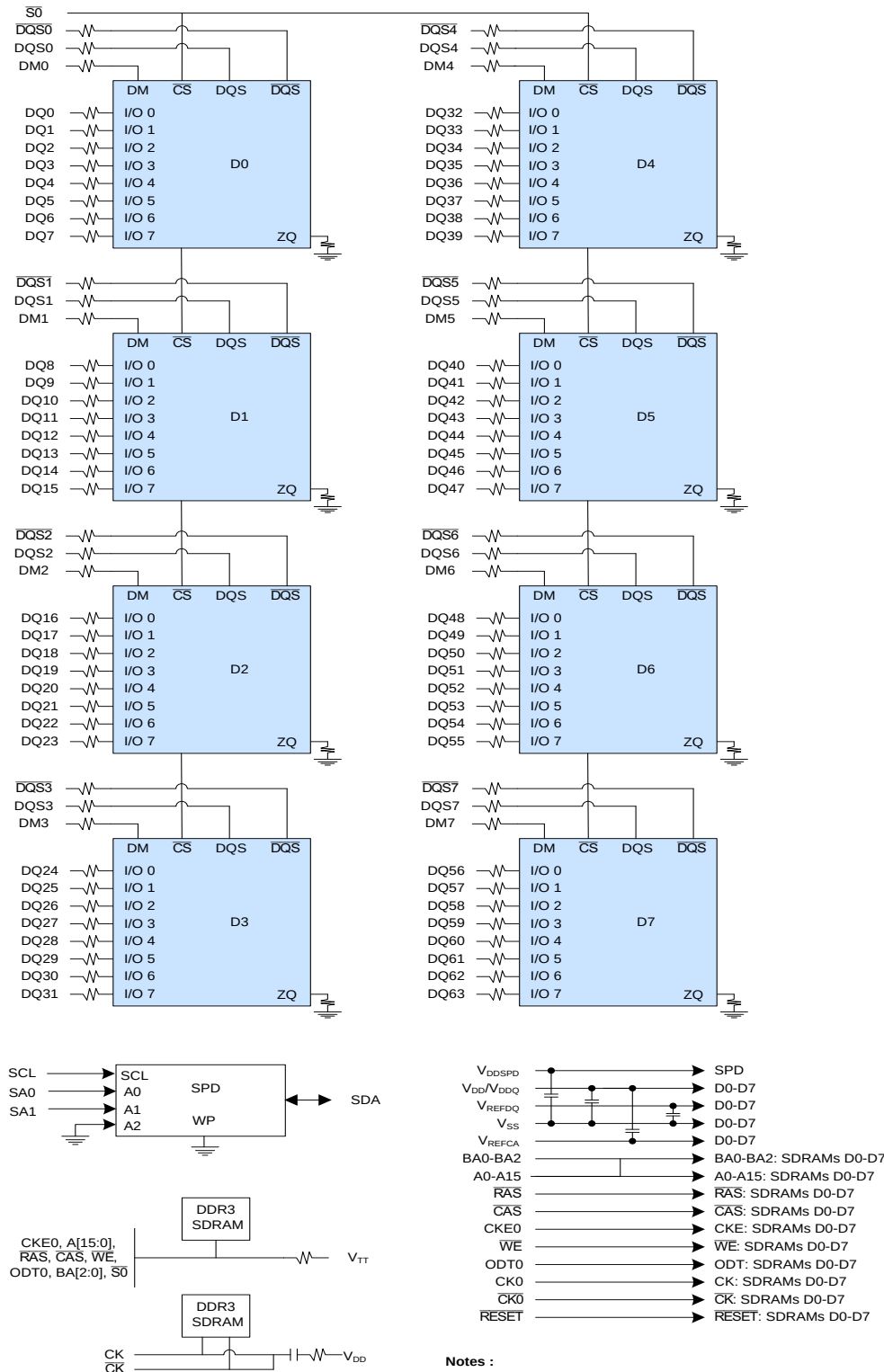
Symbol	Type	Polarity	Function
CK0, CK1 CK0, CK1	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE[1:0]	Input	Active High	Activates the DDR3 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S}$ [1:0]	Input	Active Low	Enables the associated DDR3 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue, Rank 0 is selected by $\overline{S0}$; Rank 1 is selected by $\overline{S1}$.
RAS, CAS, WE	Input	Active Low	When sampled at the positive rising edge of CK and falling edge of $\overline{CK}$, signals $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM.
ODT[1:0]	Input	Active High	Asserts on-die termination for DQ, DM, DQS, and $\overline{DQS}$ signals if enabled via the DDR3 SDRAM mode register.
BA[2:0]	Input	-	Selects which DDR3 SDRAM internal bank of eight is activated.
A[9:0] A10/AP A11 A12/ $\overline{BC}$ A[15:13]	Input	-	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA[3:0] defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[3:0] to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA[3:0] inputs. If AP is low, then BA[3:0] are used to define which bank to precharge. A12/ $\overline{BC}$ is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH, no burst chop; LOW, burst chopped).
DM[7:0]	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS[7:0] $\overline{DQS}$ [7:0]	I/O	Cross point	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR3 SDRAMs and is sent at the leading edge of the data window. DQS signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$.
DQ[63:0]	I/O	-	Data Input/Output pins.
V _{DD} , V _{DDSPD} , V _{SS}	Supply	-	Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
V _{REFDQ} , V _{REFCA}	Supply	-	Reference voltage for inputs.
SDA	I/O	-	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V _{DDSPD} on the system planar to act as a pull up.
SCL	Input	-	This pin is used to clock data into and out of the SPD EEPROM. A resistor must be connected from the SCL bus line to V _{DDSPD} on the system planar to act as a pull up.
SA[2:0]	Input	-	Address pins used to select the Serial Presence Detect.
$\overline{RESET}$	Input	-	This signal resets the DDR3 SDRAM.
ZQ	Supply	-	Reference pin for ZQ calibration.

DDR3(L) 4GB/8GB SODIMM

M2S4G64CB(C)88B4(5)N / M2S8G64CB(C)8HB4(5)N



4GB (1-Rank) Functional Block Diagram

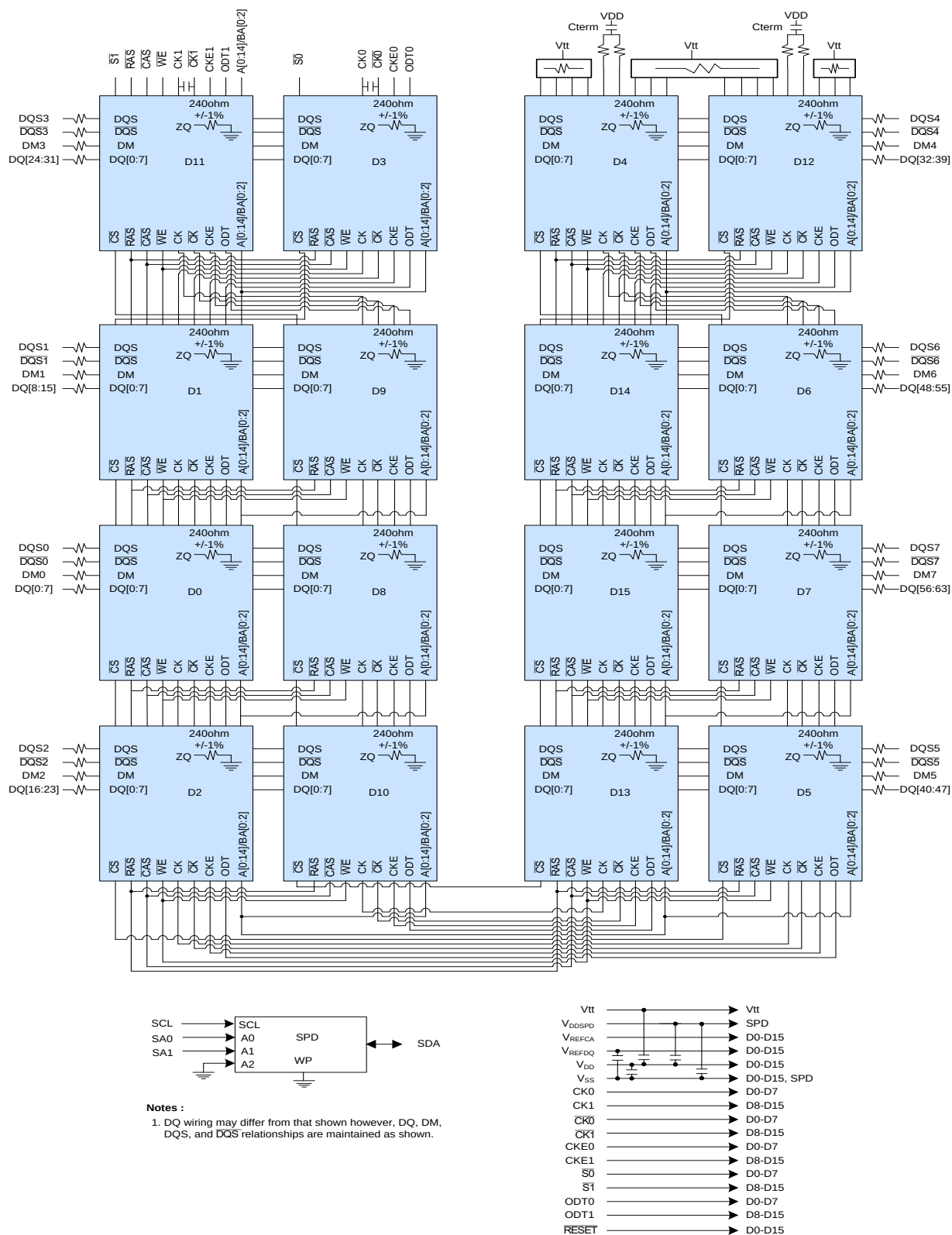


DDR3(L) 4GB/8GB SODIMM

M2S4G64CB(C)88B4(5)N / M2S8G64CB(C)8HB4(5)N



8GB (2-Ranks) Functional Block Diagram



DDR3(L) 4GB/8GB SODIMM

M2S4G64CB(C)88B4(5)N / M2S8G64CB(C)8HB4(5)N



DDR3L Operating, Standby, and Refresh Currents

Symbol	Parameter/Condition	4GB	8GB	Unit
IDD0	Operating One Bank Active-Precharge Current	660	1206	mA
IDD1	Operating One Bank Active-Read-Precharge Current	792	1338	mA
IDD2P0	Precharge Power-Down Current Slow Exit	220	440	mA
IDD2P1	Precharge Power-Down Current Fast Exit	326	651	mA
IDD2Q	Precharge Quiet Standby Current	414	827	mA
IDD2N	Precharge Standby Current	414	827	mA
IDD3P	Active Power-Down Current	440	880	mA
IDD3N	Active Standby Current	546	1091	mA
IDD4R	Operating Burst Read Current	1584	2130	mA
IDD4W	Operating Burst Write Current	1672	2218	mA
IDD5B	Burst Refresh Current	1786	2332	mA
IDD6	Self Refresh Current: Normal Temperature Range	220	440	mA
IDD7	Operating Bank Interleave Read Current	2358	2904	mA

DDR3 Operating, Standby, and Refresh Currents

Symbol	Parameter/Condition	4GB	8GB	Unit
IDD0	Operating One Bank Active-Precharge Current	704	1250	mA
IDD1	Operating One Bank Active-Read-Precharge Current	880	1426	mA
IDD2P0	Precharge Power-Down Current Slow Exit	220	440	mA
IDD2P1	Precharge Power-Down Current Fast Exit	352	704	mA
IDD2Q	Precharge Quiet Standby Current	440	880	mA
IDD2N	Precharge Standby Current	440	880	mA
IDD3P	Active Power-Down Current	528	1056	mA
IDD3N	Active Standby Current	546	1091	mA
IDD4R	Operating Burst Read Current	1646	2191	mA
IDD4W	Operating Burst Write Current	1698	2244	mA
IDD5B	Burst Refresh Current	1786	2332	mA
IDD6	Self Refresh Current: Normal Temperature Range	220	440	mA
IDD7	Operating Bank Interleave Read Current	2464	3010	mA

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit	Note
T _{OPER}	Operating Temperature (ambient)	0 to 65	°C	1
T _{STG}	Storage Temperature	-50 to 100	°C	1

Note:

- Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter		Rating			Unit	Note
			Min.	Typ.	Max.		
VDDSPD	Core Supply Voltage	—	3.0	3.3	3.6	V	
VDD	Supply Voltage	DDR3	1.425	1.5	1.575	V	1,2
		DDR3L	1.283	1.35	1.45		3,4,5,6
VDDQ	Supply Voltage for Output	DDR3	1.425	1.5	1.575	V	1,2
		DDR3L	1.283	1.35	1.45		3,4,5,6

Note:

- Under all conditions VDDQ must be less than or equal to VDD.
- VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
- Maximum DC value may not be greater than 1.425V. The DC value is the linear average of VDD/ VDDQ(t) over a very long period of time (e.g., 1 sec).
- If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
- Under these supply voltages, the device operates to this DDR3L specification.
- Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3L operation.
- VDD= VDDQ= 1.35V (1.283 – 1.45V)
Backward compatible to VDD= VDDQ= 1.5V ±0.075V
Supports DDR3L devices to be backward compatible in 1.5V applications

DDR3(L) 4GB/8GB SODIMM

M2S4G64CB(C)88B4(5)N / M2S8G64CB(C)8HB4(5)N



Revision History

Version	Page	Modified	Description	Released
1.0	-	-	Official Release.	04/2014



<http://www.elixir-memory.com/>