Rev. 1.0. Jan. 2017

MZ1KW480HMHQ-00003
MZ1KW960HMJP-00003
MZ1KW1T9HMLS-00003

M.2 NVMe PCIe SSD Specification
(SM963)

datasheet

SAMSUNG

Revision History

Revision No.	History	Draft Date	Remark	Editor by	Review by
1.0	1. Initial issue.	Jan. 26, 2017	Final	H.I. Choi	I.Y. Kim

Part Number	Capacity[1)]	LBA (512 Bytes size)
MZ1KW480HMHQ-00003	480GB	937,703,088
MZ1KW960HMJP-00003	960GB	1,875,385,008
MZ1KW1T9HMLS-00003	1.92TB	3,750,748,848

FEATURES

· PCI Express Gen3
  - Single port X4 lanes
· Compliant with PCI Express CEM Specification Rev. 3.0
· Compliant with PCI Express Base Specification Rev. 3.0
· Compliant with NVM Express Specification Rev. 1.2(Partial)
· Enhanced Power-Loss Data Protection
· End-to-End Data Protection
· Support SSD Enhanced S.M.A.R.T. Feature Set
· Static and Dynamic Wear Leveling
· RoHS / Halogen-Free Compliant

DRIVE CONFIGURATION

· Form Factor: M.2
· Interface: PCI Express Gen3 x4
· Bytes per Sector: 512, 4096 Bytes

PERFORMANCE SPECIFICATIONS[2)]

· Data Transfer Rate (128KB data size)
  - Sequential Read: Up to 2100 MB/s[3]
  - Sequential Write: Up to 1400 MB/s[3]

· Data I/O Speed (4KB data size, Sustained)
  - Random Read: Up to 430K IOPS
  - Random Write: Up to 40K IOPS

· Latency (Sustained workload)
  - Random Read/ Write (typical)[4]: 85/50us
  - Sequential Read/ Write (typical)[5]: 45/15us
  - Drive Ready Time (typical): 10s

RELIABILITY SPECIFICATIONS

· Uncorrectable Bit Error Rate: 1 sector per 10^{17} bits read
· MTBF: 2,000,000 hours
· Component Design Life: 5 years
· Endurance
  - 1.92TB/960GB/480GB: 3.6 DWPD
· TBW (@4KB Random Write)
  - 1.92TB: 12614 TB
  - 960GB: 6307 TB
  - 480GB: 3153 TB
· Data Retention: 3 months

ENVIRONMENTAL SPECIFICATIONS

· Temperature, Case (Tc[6])
  - Operating: 0 ~ 70 °C
  - Non-operating: -40 ~ 85 °C
· Humidity (non-condensing): 5 ~ 95%
· Linear Shock (0.5ms duration with 1/2 sine wave)
  - Non-operating: 1,500 Gpeak
· Vibration
  - Non-operating (20 ~ 2,000 Hz, Sinusoidal): 20 Gpeak

POWER REQUIREMENTS

· Supply Voltage / Tolerance: 3.3V±5%
· Active[7] (max. RMS): 7.5 W
· Idle (typ.): 2.5 W

PHYSICAL DIMENSION

· Width: 22.00 ± 0.15 mm
· Length: 110.00 ± 0.15 mm
· Height
  - Top: 2.00mm Max.
  - Bottom: 1.50mm Max.
· Weight: Up to 20 g

OPERATING SYSTEMS

Windows Server 2016
RHEL 7.2
CentOS 7.2
Ubuntu 15.10
Oracle Linux 7.2
SLES 12

NOTE: *Specifications are subject to change without notice.*

1) 1MB = 1,000,000 Bytes, 1GB = 1,000,000,000 Bytes, unformatted Capacity. User accessible capacity may vary depending on operating environment and formatting.
2) Based on PCI Express Gen3 x4, Random performance measured using FIO 2.1.3 in Linux RHEL 6.6(Kernel 3.14.29) with 4KB (4,096 bytes) of data transfer size in queue depth 32 by 4 workers and Sequential performance with 128KB (131,072 bytes) of data transfer size in queue depth 32 by 1 worker. Actual performance may vary depending on use conditions and environment.
3) 1 MB/sec = 1,048,576 bytes/sec was used in sequential performance.
4) The random latency is measured by using FIO 2.1.3 in Linux RHEL 6.6 (Kernel 3.14.29) and 4KB (4,096 bytes) transfer size with queue depth 1 by 1 worker.
5) The Sequential latency is measured by using FIO 2.1.3 in Linux RHEL 6.6 (Kernel 3.14.29) and 4KB (4,096 bytes) transfer size with queue depth 1 by 1 worker.
6) Tc is measured at the hottest point on the case. Sufficient airflow is recommended to be operated properly on heavier workloads wthin device operating temperature.
7) Active power is measured using IOMeter2006 on Windows Server 2012.

Table Of Contents

1.0 Introduction

1.1 General Description

This document describes the specifications of the Samsung SSD SM963, which is a native-PCIe SSD for enterprise application.

The Samsung SSD SM963 presents outstanding performance with instant responsiveness to the host system, by applying the Peripheral Component Interconnect Express (PCIe) 3.0 interface standard, as well as highly efficient Non-Volatile Memory Express (NVMe) Protocol.

The Samsung SSD SM963 delivers wide bandwidth of up to 2.1GB/s for sequential read speed and up to 1.4GB/s for sequential write speed under up to 7.5W power. The Samsung SSD SM963 delivers random performance of up to 430KIOPS for random 4KB read and up to 40KIOPS for random 128KB write in the sustained state.

By combining the enhanced reliability Samsung NAND Flash memory silicon with NAND Flash management technologies, the Samsung SSD SM963 delivers the extended endurance of up to 3.6 drive writes per day over 5 years, which is suitable for enterprise applications, in M.2 form factor lineups: 480GB, 960GB, 1.92TB.

In addition, the Samsung SSD SM963 supports Power Loss Protection (PLP). PLP solution can guarantee that data issued by the host system are written to the storage media without any loss in the event of sudden power off or sudden power failure.

1.2 Product List

[Table 1] Product List

Type	Capacity	Part Number
M.2[1)]	480GB	MZ1KW480HMHQ-00003
	960GB	MZ1KW960HMJP-00003
	1.92TB	MZ1KW1T9HMLS-00003

NOTE:
1) 22.00(±0.15) x 110.00(±0.15)

1.3 Ordering Information

M Z X X X X X X X X X X - X X X X X
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

1. Memory (M)

2. SSD (Z)

3. Interface/Form Factor
1: PCIe M.2 (22x110)

4. Line-Up
K: Client/SV (VNAND 2bit MLC)

5. SSD CTRL
W: Polaris

6~8. SSD Density
480: 480GB
960: 960GB
1T9: 1.92TB

9. NAND PKG
H: BGA (LF,HF)

10. Flash Generation
M: 1st Generation

11~12. NAND Density
HQ: 1T QDP 4CE
JP: 2T ODP 8CE
LS: 4T HDP 2CE(FBI)

13. " - "

14. PCB Type
0: None

15. HW revision
0: No revision

16. Packing type
0: Bulk

17~18. Customer
03: General

2.0 PRODUCT SPECIFICATIONS

2.1 Capacity

[Table 2] User Capacity and Addressable Sectors

Capacity[2)]	Max LBA[3)]
480GB	937,703,088
960GB	1,875,385,008
1.92 TB	3,750,748,848

NOTE:
1) Gigabyte (GB) = 1,000,000,000 Bytes, 1 Sector = 512Bytes
2) Capacity shown represents the total usable capacity of the SSD which may be less than the total physical capacity. A certain area in physical capacity, not in the area shown to the user, might be used for the purpose of NAND flash management.
3) Max. LBA shown represents the total user addressable sectors in LBA mode and calculated by IDEMA rule.

2.2 Performance

[Table 3] Sustained Random Read/Write Performance (IOPS)

Maximum Performance[1)]	Unit	480GB	960GB	1.92TB
Random 4KB Read	IOPS	280K	430K	430K
Random 4KB Write	IOPS	23K	33K	40K

NOTE:
1) Random performance was measured by using FIO 2.1.3 in Linux RHEL 6.6(Kernel 3.14.29) with 4KB (4,096 bytes) of data transfer size in Queue Depth=32 by 4 workers. Measurements were performed on a full Logical Block Address (LBA) span of the drive in sustained state. The actual performance may vary depending on use conditions and environment.

[Table 4] Sequential Read/Write Performance

Maximum Performance[1)]	Unit	480GB	960GB	1.92TB
Sequential 128KB Read	MB/s	1200	2000	2100
Sequential 128KB Write	MB/s	900	1400	1400

NOTE:
1)Sequential performance was measured by using FIO 2.1.3 in Linux RHEL 6.6(Kernel 3.14.29) with 128KB (131,072 bytes) of data transfer size in Queue Depth=32 by 1 worker.
2) 1 MB/sec = 1,048,576 bytes/sec was used in sequential performance.

2.3 Latency

[Table 5] Latency[1] (sustained state)

Queue Depth = 1	Unit	480GB	960GB	1.92TB
Random Read/Write[2]	us	85 / 50	85 / 50	85 / 50
Sequential Read/Write[3]	us	15 / 45	15 / 45	15 / 45
Drive Ready Time[4]	sec	10	10	10

NOTE:
1) Typical values
2) The random latency is measured by using FIO 2.1.3 in Linux RHEL 6.6(Kernel 3.14.29) and 4KB transfer size with queue depth 1 by 1 worker.
3) The sequential latency is measured by using FIO 2.1.3 in Linux RHEL 6.6(Kernel 3.14.29) and 4KB transfer size with queue depth 1 by 1 worker.
4) The maximum taking time to be ready for receiving commands after power-up (CSTS.Ready=1). It is expected that I/O commands may not be completed at this point.

2.4 Quality of Service (QoS)

[Table 6] Quality of Service (QoS)

Quality of Service (99%)	Unit	480GB	960GB/1.92TB
Read(4KB)(QD=1)	ms	0.1	0.1
Write(4KB)(QD=1)	ms	0.1	0.1
Read(4KB)(QD=32)	ms	0.7	0.5
Write(4KB)(QD=32)	ms	1.6	1.6

Quality of Service (99.99%)	Unit	480GB	960GB/1.92TB
Read(4KB)(QD=1)	ms	0.2	0.2
Write(4KB)(QD=1)	ms	0.2	0.2
Read(4KB)(QD=32)	ms	1.3	0.8
Write(4KB)(QD=32)	ms	1.6	1.6

NOTE:
1) 1. QoS is measured using Fio 2.1.3 (99 and 99.99%) in Linux RHEL 6.6 (Kernel 3.14.29) with queue depth 1, 32 on 4KB random read and write.
2) QoS is measured as the maximum round-trip time taken for 99 and 99.99% of commands to host.

2.5 Power

The Samsung SSD SM963 is implemented in standardized M.2 form factor and gets primary 3.3V power t from the host system.
For 3.3V, the allowable voltage tolerance and noise level in SSD are described in chapter 2.5.1, the power consumption in 2.5.2 and the inrush current in 2.4.3.

2.5.1 Maximum Voltage Ratings (3.3V)

[Table 7] Allowable Voltage Tolerance[1]

Operating Voltage	480GB	960GB	1.92TB
Allowable Voltage	3.3V±5%		
Allowable noise/ripple	3.3V±5%		

NOTE:
1) The components inside SSD were designed to endure the range of voltage fluctuations, which might be induced by the host system.

2.5.2 Power Consumption (3.3V)

In enterprise server and storage system, the Samsung SSD SM963 is designed for the specific usage, which means that SSD will be always operated by the host system during the entire life. Hence, the Samsung SSD SM963 does not manage any low power modes except for the Active/Idle and Off mode.

[Table 8] Power Consumption (3.3V Supply Voltage)[1]

Power Mode		480GB	960GB	1.92TB
Active[2]	Read	5.4W	7.1W	7.5W
	Write	5.0W	6.4W	6.5W
Idle[3]		2.4W	2.4W	2.4W
Off		0W	0W	0W

NOTE:
1) Power consumption was measured in the 3.3V power pins of the connector plug in SSD. The active and idle power is defined as the highest averaged power value, which is the maximum RMS average value over 100 ms duration.
2) The measurement condition for active power is assumed for 100% sequential read and write.
3) The idle state is defined as the state that the host system can issue any commands into SSD at any time.

2.5.3 Inrush Current

[Table 9] Inrush Current

Inrush Current	480GB	960GB	1.92TB
3.3 V	3.0 A[1]		

NOTE:
1) The measurement value of inrush current is also compatible with the standard specification of “PCIe M.2 Electromechanical spec 1.1” released by PCI-SIG.

2.5.4 Power Loss Protection

By using internal back-up power technology, the Samsung SSD SM963 supports power loss protection (PLP) feature to guarantee the reliability of data requested by the host system. When power is unpredictably lost, SSD can detect automatically this abnormal situation and transfer all user data and meta-data cached in DRAM into the Flash media during any SSD operations.

2.6 Reliability

The reliability specification of the Samsung SSD SM963 follows JEDEC standard, which are included in JESD218A and JESD219A documents

2.6.1 Mean Time Between Failures

By definition, Mean Time between Failures (MTBF) is the estimated time between failures occurring during SSD operation.

[Table 10] MTBF Specifications

Parameter	480GB	960GB	1.92TB
MTBF	2,000,000 Hours		

2.6.2 Uncorrectable Bit Error Rate

By definition, Uncorrectable Bit Error Rate (UBER) is a metric for the rate of occurrence of data errors, equal to the number of data errors per bits read as specified in the JESD218 document of JEDEC standard.

[Table 11] UBER Specifications

Parameter	480GB	960GB	1.92TB
UBER	1 sector per 10^{17} bits read		

2.6.3 Data Retention

By definition, data retention is the expected time period for retaining data in the SSD at the maximum rated endurance in power-off state as specified in the JESD218 document of JEDEC standard.

[Table 12] Data Retention

Parameter	480GB	960GB	1.92TB
Data Retention[1]	3 months		

NOTE:
1) Data retention was measured by assuming that SSD reaches the maximum rated endurance at 40C in power-off state.

2.6.4 Endurance

By definition, the endurance of SSD in enterprise application is defined as the maximum number of drive writes per day that can meet the requirements specified in the JESD218 document of JEDEC standard.

[Table 13] Drive Write Per Day (DWPD)

Parameter	480GB	960GB	1.92TB
DWPD	3.6 drive writes per day over 5 years		

[Table 14] Data Retention

Parameter	Unit	480GB	960GB	1.92TB
TBW	TB	3153	6307	12614

2.7 Environmental Specification

2.7.1 Temperature

[Table 15] Temperature, Case (Tc[1])

Parameter		480GB	960GB	1.92TB
Temperature[1]	Operating	0 to 70°C		
	Non-operating	-40 to 85°C		

NOTE:
1) Tc is measured at the surface of NAND Flash package. Sufficient airflow is recommended to be operated properly on heavier workloads wthin device operating temperature.

2.7.2 Humidity

[Table 16] Humidity

Parameter		480GB	960GB	1.92TB
Humidity[1]	Non-operating	5% to 95%		

NOTE:
1) Humidity is measured in non-condensing state.

2.7.3 Shock and Vibration

[Table 17] Shock and Vibration

Parameter		480GB	960GB	1.92TB
Shock[1]	Non-operating	1,500 G		
Vibration[2]	Non-operating	20 Gpeak		

NOTE:
1) Test condition for shock: 0.5ms duration with half sine wave.
2) Test condition for vibration: 20Hz to 2000Hz, Sinusoidal.

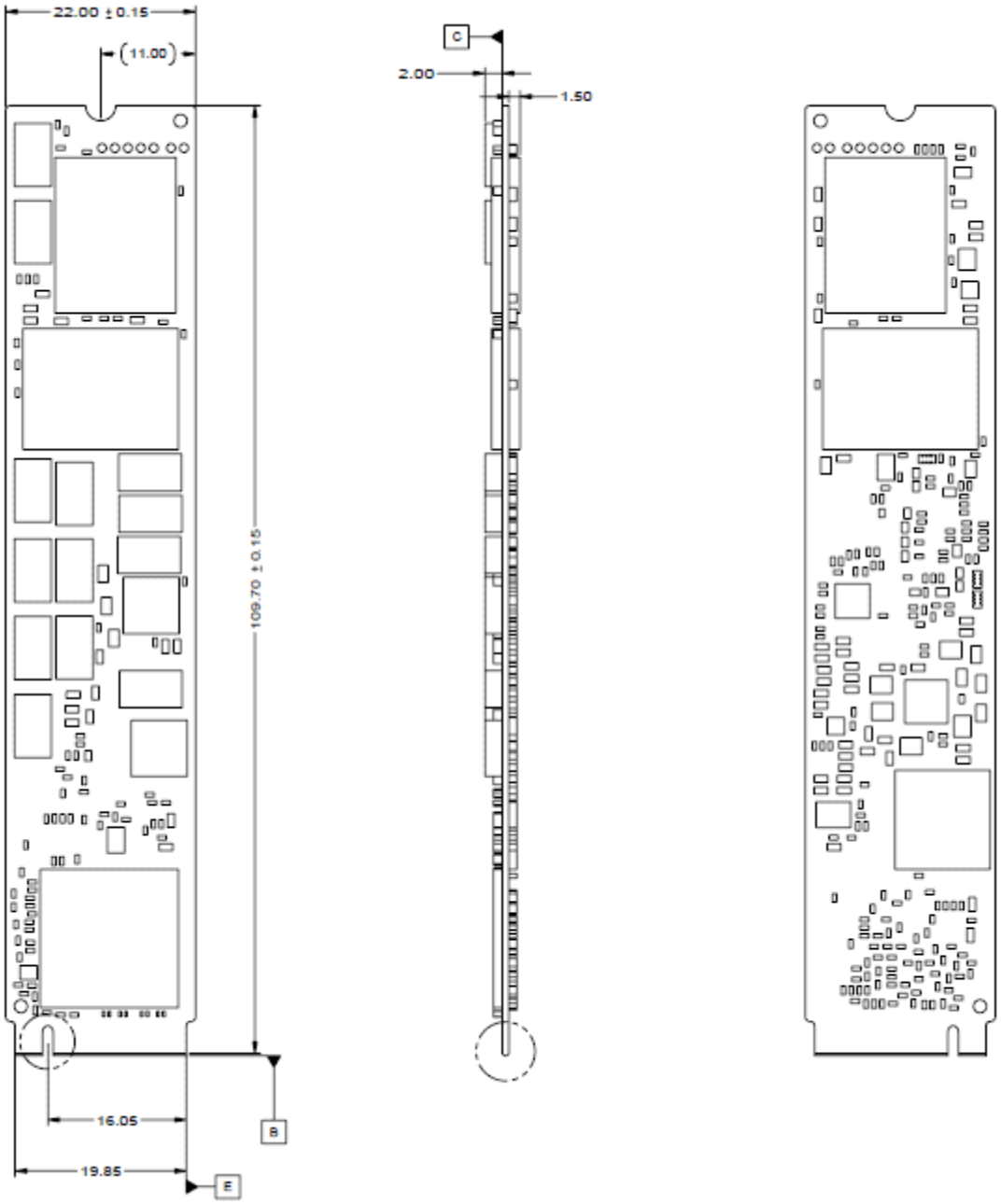
3.0 Mechanical Specifications

3.1 Physical Information

The physical dimension of the Samsung SSD SM963 M.2 form factor follows the standardized dimensions defined by PCI Express M.2 Specification

[Table 18] Physical Dimensions and Weight

Parameter	Unit	480GB	960GB	1.92TB
Width	mm	22.00 ± 0.15		
Length	mm	110.00 ± 0.15		
Thickness	mm	Top 2.00mm max Bottom 1.50mm max		
Weight	g	Up to 20g		



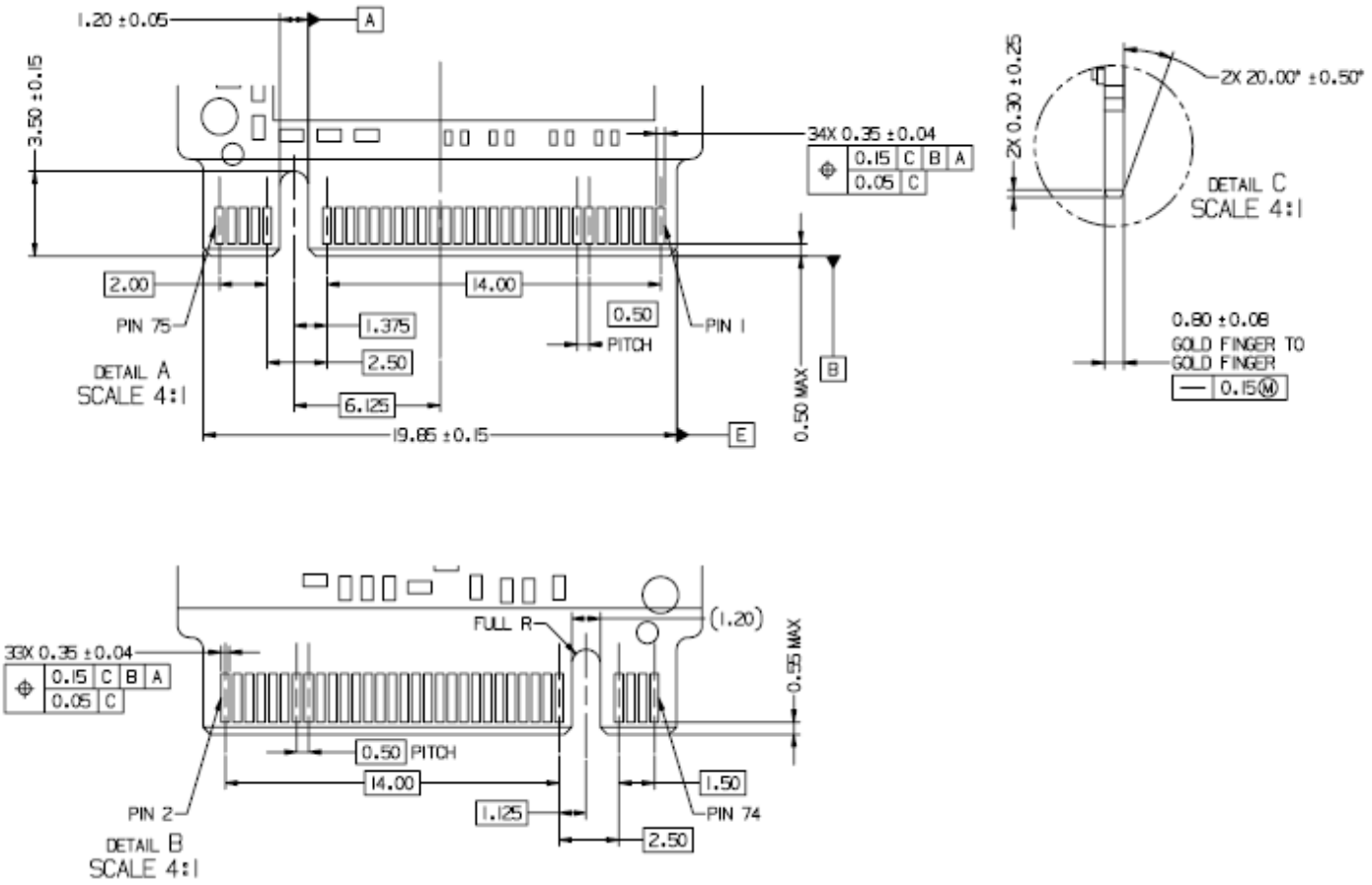


Figure 1. Mechanical Outline

4.0 Interface Specification

4.1 Connector Dimensions

[TOP VIEW] [BOTTOM VIEW]

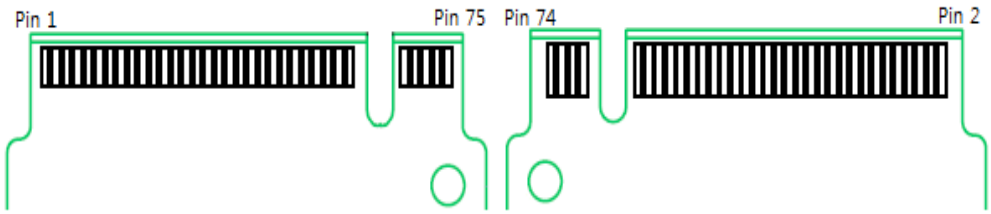


Figure 2. M.2 Signal and Power pins

4.2 Connector Pin Assignments

[Table 19] Certifications and Declarations

Pin #	Assignment	Description	Pin #	Assignment	Description
74	3.3 V	Primary Power	75	GND	Ground
72	3.3 V	Primary Power	73	GND	Ground
70	3.3 V	Primary Power	71	GND	Ground
68	SUSCLK	Floated	69	PEDET(NC-PCIe)	Floated
58	Reserved for MFG CLOCK	Floated	67	Not Used	
56	Reserved for MFG DATA	Floated	57	GND	Ground
54	PEWAKE#	Floated	55	REFCLKp	PCIe Reference Clock +
52	CLKREQ#		53	REFCLKn	PCIe Reference Clock -
50	PERST#		51	GND	Ground
48	Not Used	Floated	49	PERp0	PCIe Receive- (lane 0)
46	Not Used		47	PERn0	PCIe Receive+ (lane 0)
44	ALERT#	SMBUS_alert	45	GND	Ground
42	SMDAT	SMBUS_data	43	PETp0	PCIe Transmit+ (lane 0)
40	SMCLK	SMBUS_clock	41	PETn0	PCIe Transmit- (lane 0)
38	Not Used		39	GND	Ground
36	Not Used		37	PERp1	PCIe Receive- (lane 1)
34	Not Used		35	PERn1	PCIe Receive+ (lane 1)
32	Not Used		33	GND	Ground
30	Not Used		31	PETp1	PCIe Transmit+ (lane 1)
28	Not Used		29	PETn1	PCIe Transmit- (lane 1)
26	Not Used		27	GND	Ground
24	Not Used		25	PERp2	PCIe Receive- (lane 2)
22	Not Used		23	PERn2	PCIe Receive+ (lane 2)
20	Not Used		21	GND	Ground
18	3.3 V	Primary Power	19	PETp2	PCIe Transmit+ (lane 2)
16	3.3 V	Primary Power	17	PETn2	PCIe Transmit- (lane 2)
14	3.3 V	Primary Power	15	GND	Ground
12	3.3 V	Primary Power	13	PERp3	PCIe Receive- (lane 3)
10	LED1#	Drive Active Signal (Optional, Refer to [Table 20])	11	PERn3	PCIe Receive+ (lane 3)
8	Not Used		9	GND	Ground
6	Not Used		7	PETp3	PCIe Transmit+ (lane 3)
4	3.3 V	Primary Power	5	PETn3	PCIe Transmit- (lane 3)
2	3.3 V	Primary Power	3	GND	Ground
			1	GND	Ground

[Table 20] Simple Indicator Protocol for Device Activity (Pin 10, Optional)

Device State	Pin Out
Active	Toggle
Idle	High[1)]

NOTE:
1) DAS/LED Pin is toggle when host initiated Background job

5.0 PCI and NVM Express Registers

5.1 PCI Express Registers

5.1.1 PCI Register Summary

[Table 21] PCI Register Summary

Start Address	End Address	Name	Type
00h	3Fh	PCI Header	PCI Capability
40h	47h	PCI Power Management Capability	PCI Capability
50h	67h	MSI Capability	PCI Capability
70h	A3h	PCI Express Capability	PCI Capability
B0h	BBh	MSI-X Capability	PCI Capability
100h	12Bh	Advanced Error Reporting Capability	PCI Capability
148h	153h	Device Serial No Capability	PCI Capability
158h	167h	Power Budgeting Capability	PCI Capability
168h	17Bh	Secondary PCI Express Header	PCI Capability
188h	18Fh	Latency Tolerance Reporting (LTR)	PCI Capability
190h	19Fh	L1 Substates Capability Register	PCI Capability

5.1.2 PCI Header Registers

[Table 22] PCI Header Register Summary

Start Address	End Address	Symbol	Description
00h	03h	ID	Identifiers
04h	05h	CMD	Command Register
06h	07h	STS	Device Status
08h	08h	RID	Revision ID
09h	0Bh	CC	Class Codes
0Ch	0Ch	CLS	Cache Line Size
0Dh	0Dh	MLT	Master Latency Timer
0Eh	0Eh	HTYPE	Header Type
0Fh	0Fh	BIST	Built in Self Test
10h	13h	MLBAR (BAR0)	Memory Register Base Address (lower 32-bit)
14h	17h	MUBAR (BAR1)	Memory Register Base Address (upper 32-bit)
18h	1Bh	IDBAR (BAR2)	Index/Data Pair Register Base Address
1Ch	1Fh	BAR3	Reserved
20h	23h	BAR4	Reserved
24h	27h	BAR5	Reserved
28h	2Bh	CCPTR	CardBus CIS Pointer
2Ch	2Fh	SS	Subsystem Identifiers
30h	33h	EROM	Expansion ROM Base Address
34h	34h	CAP	Capabilities Pointer
35h	3Bh	RO	Reserved
3Ch	3Dh	INTR	Interrupt Information
3Eh	3Eh	MGNT	Minimum Grant
3Fh	3Fh	MLAT	Maximum Latency

[Table 23] Identifier Register

Bits	Type	Default Value	Description
31:16	RO	A804h	Device ID
0:15	RO	144Dh	Vendor ID

[Table 24] Command Register

Bits	Type	Default Value	Description
15:11	RO	0	Reserved
10	RW	0	Interrupt Disable
9	RO	0	Fast Back-to-Back Enable (N/A)
8	RW	0	SERR# Enable (N/A)
7	RO	0	IDSEL Stepping/Wait Cycle Control (N/A)
6	RW	0	Parity Error Response Enable
5	RO	0	VGA Palette Snooping Enable (N/A)
4	RO	0	Memory Write and Invalidate Enable (N/A)
3	RO	0	Special Cycle Enable (N/A)
2	RW	0	Bus Master Enable
1	RW	0	Memory Space Enable
0	RW	0	I/O Space Enable

[Table 25] Device Status Register

Bits	Type	Default Value	Description
15	RW1C	0	Detected Parity Error
14	RW1C	0	Signaled System Error (N/A)
13	RW1C	0	Received Master Abort
12	RW1C	0	Received Target Abort
11	RW1C	0	Signaled Target Abort
10:9	RO	0	DEVSEL Timing (N/A)
8	RW1C	0	Master Data Parity Error Detected
7	RO	0	Fast Back-to-Back Transaction Capable (N/A)
6	RO	0	Reserved
5	RO	0	66MHz Capable (N/A)
4	RO	1	Capabilities List
3	RO	0	INTx Status
2:0	RO	0	Reserved

[Table 26] Revision ID Register

Bits	Type	Default Value	Description
7:0	RO	00h	Controller Hardware Revision ID

[Table 27] Class Code Register

Bits	Type	Default Value	Description
23:16	RO	1h	Base Class Code
15:8	RO	8h	Sub Class Code
7:0	RO	2h	Programming Interface

[Table 28] Cache Line Size Register

Bits	Type	Default Value	Description
7:0	RW	0h	N/A

[Table 29] Master Latency Timer Register

Bits	Type	Default Value	Description
7:0	RO	0	N/A

[Table 30] Header Type Register

Bits	Type	Default Value	Description
7:0	RO	0	N/A

[Table 31] Built In Self Test Register

Bits	Type	Default Value	Description
7:0	RO	0	N/A

[Table 32] Memory Register Base Address Lower 32-bits (BAR0) Register

Bits	Type	Default Value	Description
31:14	RW	0	Base Address
13:4	RO	0	
3	RO	0	Pre-Fetchable
2:1	RO	2	Address Type (64-bit)
0	RO	0	Memory Space Indicator (MEMSI)

[Table 33] Memory Register Base Address Upper 32-bits (BAR1)

Bits	Type	Default Value	Description
31:0	RW	0	Base Address

[Table 34] Index/Data Pair Register Base Address (BAR2) Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 35] BAR3 Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 36] Vendor Specific BAR4 Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 37] Vendor Specific BAR5 Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 38] Cardbus CIS Pointer Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 39] Subsystem Identifier Register

Bits	Type	Default Value	Description
31:16	RO	A801	Subsystem ID
15:0	RO	144D	Subsystem Vendor ID

[Table 40] Expansion ROM Register

Bits	Type	Default Value	Description
31:17	RW	0	Expansion ROM Base Address
16:1	RO	0	
0	RW	0	Expansion ROM Enable/Disable

[Table 41] Capabilities Pointer Register

Bits	Type	Default Value	Description
7:0	RO	40h	Capability Pointer (Points to PCI Power Management Capability Offset)

[Table 42] Interrupt Information Register

Bits	Type	Default Value	Description
15:8	RO	01	Interrupt Pin
7:0	RW	FF	Interrupt Line

[Table 43] Minimum Grant Register

Bits	Type	Default Value	Description
7:0	RO	0	Minimum Grant

[Table 44] Maximum Latency Register

Bits	Type	Default Value	Description
7:0	RO	0	Maximum Latency

5.1.3 PCI Power Management Registers

[Table 45] PCI Power Management Capability Register Summary

Start Address	End Address	Symbol	Description
40h	40h	PID	PCI Power Management Capability ID
41h	41h	Next cap ptr	Next cap ptr
42h	43h	PMC	PC Power Management Capabilities
44h	45h	PMCS	PCI Power Management Control and Status
46h	46h	PMCSR_BSE	PMCSR_BSE Bridge Extensions
47h	47h	Data	Data

[Table 46] PCI Power Management Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	50h	Next Capability
7:0	RO	1h	Capability ID

[Table 47] PCI Power Management Capability Register

Bits	Type	Default Value	Description
15:11	RO	0	PME Support (N/A)
10	RO	0	D2 Support
9	RO	0	D1 Support
8:6	RO	0	AUX Current (N/A)
5	RO	0	Device Specific Initialization
4	RO	0	Reserved
3	RO	0	PME Clock
2:0	RO	3h	Version (Support for revision 1.2)

[Table 48] PCI Power Management Control and Status Register

Bits	Type	Default Value	Description
31:24	RO	0	data register
23	RO	0	Bus power/Clock enable
22	RO	0	B2, B3 support
21:16	RsvdP	0	Reserved
15	RW1CS	0	PME_Status (N/A)
14:13	RO	0	Data Scale (N/A)
12:09	RO	0	Data Select (N/A)
8	RWS	0	PME enable (N/A)
7:04	RsvdP	0	Reserved
3	RO	1	No Soft Reset
2	RsvdP	0	Reserved
1:00	RW	0	Power State

5.1.4 Message Signaled Interrupt Registers

[Table 49] Message Signaled Interrupt Capability Register Summary

Start Address	End Address	Symbol	Description
50h	51h	MID	Message Signaled Interrupt Capability ID
52h	53h	MC	Message Signaled Interrupt Message Control
54h	57h	MA	Message Signaled Interrupt Message Address
58h	5Bh	MUA	Message Signaled Interrupt Upper Address
5Ch	5Dh	MD	Message Signaled Interrupt Message Data
60h	63h	MMASK	Message Signaled Interrupt Mask Bits
64h	67h	MPEND	Message Signaled Interrupt Pending Bits

[Table 50] Message Signaled Interrupt Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	70h	Next Capability
7:0	RO	05h	Capability ID

[Table 51] Message Signaled Interrupt Control Register

Bits	Type	Default Value	Description
15:9	RsvdP	0	Reserved
8	RO	0	Per Vector Masking Capable
7	RO	1h	64-bit Address Capable
6:4	RW	0h	Multiple Message Enable
3:1	RO	5h	Multiple Message Capable
0	RW	0h	MSI Enable

[Table 52] Message Signaled Interrupt Lower Address Register

Bits	Type	Default Value	Description
31:2	RW	0	Address
1:0	RO	0	Reserved

[Table 53] Message Signaled Interrupt Upper Address Register

Bits	Type	Default Value	Description
31:0	RW	0	Upper Address

[Table 54] Message Signaled Interrupt Message Data Register

Bits	Type	Default Value	Description
16:31	RsvdP	0	Reserved
0:15	RO	0	Data

[Table 55] Message Signaled Interrupt Mask Bits Register

Bits	Type	Default Value	Description
31:0	RW	0	Mask Bits

[Table 56] Message Signaled Interrupt Pending Bits Register

Bits	Type	Default Value	Description
31:0	RO	0	Pending Bits

5.1.5 MSI-X Registers

[Table 57] MSI-X Capability Register Summary

Start Address	End Address	Symbol	Description
B0h	B1h	MXID	MSI-X Capability ID
B2h	B3h	MXC	MSI-X Message Control
B4h	B7h	MTAB	MSI-X Table Offset and Table BIR
B8h	BBh	MPBA	MSI-X PBA Offset and PBA BIR

[Table 58] MSI-X Identifier Register

Bits	Type	Default Value	Description
15:8	RO	00h	Next Capability
7:0	RO	11h	Capability ID

[Table 59] MSI-X Control Register

Bits	Type	Default Value	Description
15	RW	0	MSI-X Enable
14	RW	0	Function Mask
13:11	RsvdP	0	Reserved
10:0	RO	7h	Table Size

[Table 60] MSI-X Table Offset Register

Bits	Type	Default Value	Description
31:3	RO	600h	Table Offset
2:0	RO	0	Table BIR

[Table 61] MSI-X Pending Bit Array Offset Register

Bits	Type	Default Value	Description
31:3	RO	400h	Pending Bit Array Offset
2:0	RO	0	Pending Bit Array BIR

5.1.6 PCI Express Capability Registers

[Table 62] PCI Express Capability Register Summary

Start Address	End Address	Symbol	Description
70h	71h	PXID	PCI Express Capability ID
72h	73h	PXCAP	PCI Express Capabilities
74h	77h	PXDCAP	PCI Express Device Capabilities
78h	79h	PXDC	PCI Express Device Control
7Ah	7Bh	PXDS	PCI Express Device Status
7Ch	7Fh	PXLCAP	PCI Express Link Capabilities
80h	81h	PXLC	PCI Express Link Control
82h	83h	PXLS	PCI Express Link Status
94h	97h	PXDCAP2	PCI Express Device Capabilities 2
98h	99h	PXDC2	PCI Express Device Control 2
9Ah	9Bh	PXDS2	PCI Express Device Status 2
9Ch	9Fh	PXLCAP2	PCI Express Link Capabilities 2
A0h	A1h	PXLC2	PCI Express Link Control 2
A2h	A3h	PXLS2	PCI Express Link Status 2

[Table 63] PCI Express Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	B0h	Next Pointer (MSI-X Capability)
7:0	RO	10h	Capability ID

[Table 64] PCI Express Capabilities Register

Bits	Type	Default Value	Description
15:14	RsvdP	0	Reserved
13:9	RO	0	Interrupt Message Number
8	HwInit	0	Slot Implementation (N/A)
7:4	RO	0	Device/Port Type
3:0	RO	2h	Capability Version

[Table 65] PCI Express Device Capabilities Register

Bits	Type	Default Value	Description
31:29	RsvdP	0	Reserved
28	RO	1	Function Level Reset Capability
27:26	RO	0	Captured Slot Power Limit Scale
25:18	RO	0	Captured Slot Power Limit Value
17:16	RO	0	Reserved
15	RO	1	Role-based Error Reporting
14:12	RO	0	Reserved
11:9	RO	7h	Endpoint L1 Acceptable Latency
8:6	RO	7h	Endpoint L0 Acceptable Latency
5	RO	0	Extended Tag Field Supported
4:3	RO	0	Phantom Functions Supported
2:0	RO	1h	Max Payload Size Supported (256 byte payload)

[Table 66] PCI Express Device Control Register

Bits	Type	Default Value	Description
15	RW	0	Initiate Function Level Reset
14:12	RW	2h	Max Read Request Size
11	RW	1	Enable No Snoop
10	RWS	0	Aux Power PM Enable (N/A)
9	RW	0	Phantom Functions Enable (N/A)
8	RW	0	Extended Tag Enable
7:5	RW	0	Max Payload Size
4	RW	1	Enable Relaxed Ordering (N/A)
3	RW	0	Unsupported Request Reporting Enable
2	RW	0	Fatal Error Reporting Enable
1	RW	0	Non-Fatal Error Reporting Enable
0	RW	0	Correctable Error Reporting Enable

[Table 67] PCI Express Device Status Register

Bits	Type	Default Value	Description
15:6	RsvdP	0	Reserved
5	RO	0	Transactions Pending
4	RO	1	Aux Power Detected
3	RW1C	0	Unsupported Request Detected
2	RW1C	0	Fatal Error Detected
1	RW1C	0	Non-Fatal Error Detected
0	RW1C	0	Correctable Error Detected

[Table 68] PCI Express Link Capabilities Register

Bits	Type	Default Value	Description
31:24	HwInit	0 (Port 0)	Port Number
23	RsvdP	0	Reserved
22	HwInit	1h	ASPM Optionality Compliance
21	RO	0	Link Bandwidth Notification Capability (N/A)
20	RO	0	Data Link Layer Link Active Reporting Capable (N/A)
19	RO	0	Surprise Down Error Reporting Capable (N/A)
18	RO	0h	Clock Power Management
17:15	RO	6	L1 Exit Latency
14:12	RO	7h	L0s Exit Latency
11:10	RO	0	Active State Power Management Support
9:4	RO	4h (x4 link)	Maximum Link Width
3:0	RO	3h	Supported Link Speeds

[Table 69] PCI Express Link Control Register

Bits	Type	Default Value	Description
15:12	RsvdP	0	Reserved
11	RsvdP	0	Link Autonomous Bandwidth Interrupt Enable
10	RsvdP	0	Link Bandwidth Management Interrupt Enable
9	RsvdP	0	Hardware Autonomous Width Disable
8	RW	0	Enable Clock Power Management
7	RW	0	Extended Sync
6	RW	0	Common Clock Configuration
5	RsvdP	0	Retrain Link
4	RsvdP	0	Link Disable
3	Root Ports (RO) End Points & Bridges (RW) Switch Ports (RO)	0	Read Completion Boundary (N/A)
2	RsvdP	0	Reserved
1:00	RW	0	Active State Power Management Control

[Table 70] PCI Express Link Status Register

Bits	Type	Default Value	Description
15	RW1C	0h	Link Autonomous Bandwidth Status
14	RW1C	0	Link Bandwidth Management Status
13	RO	0	Data Link Layer Link Active
12	HwInit	1	Slot Clock Configuration
11	RO	0	Link Training (1: Link training in progress;0: No link training in progress) (Non-standard)
10	RO	0	Reserved
9:4	RO	1h	Negotiated Link Width
3:0	RO	1h	Current Link Speed

[Table 71] PCI Express Device Capabilities 2 Register

Bits	Type	Default Value	Description
31	HwInit	0	FRS Supported (N/A)
30:24	RsvdP	0	Reserved
23:22	HwInit	0	Max End-End TLP Prefixes (N/A)
21	HwInit	0	End-End TLP Prefix Supported (N/A)
20	RO	0	Extended Format Field Supported (N/A)
19:18	HwInit	0	OBFF Supported (N/A)
17:16	RsvdP	0	Reserved
15:14	HwInit	0	LN System CLS (N/A)
13:12	RO	0	TPH Completer Supported (N/A)
11	RO	1	Latency Tolerance Reporting Supported
10	HwInit	0	No RO-enabled PR-PR Passing (N/A)
9	RO	0	128-bit Atomic CAS Completer Supported (N/A)
8	RO	0	64-bit Atomic Op Completer Supported (N/A)
7	RO	0	32-bit Atomic Op Completer Supported (N/A)
6	RO	0	Atomic Op Routing Supported (N/A)
5	RO	0	ARI Forwarding Supported (N/A)
4	RO	1	Completion Timeout Disable Supported
3:0	HwInit	Fh	Completion Timeout Ranges Supported (50us to 200ms)

[Table 72] PCI Express Device Control 2 Register

Bits	Type	Default Value	Description
15	RsvdP	0	End-to-end TLP Prefix Blocking (N/A)
14:13	RW/RsvdP	0	OBFF Enable (N/A)
12:11	RsvdP	0	Reserved
10	RW	0	Latency Tolerance Reporting Mechanism Enable
9	RW	0	IDO Completion Enable (N/A)
8	RW	0	IDO Request Enable (N/A)
7	RW	0	AtomicOp Egress Blocking (N/A)
6	RW	0	AtomicOp Requester Enable (N/A)
5	RW	0	ARI Forwarding Enable
4	RW	0	Completion Timeout Disable
3:0	RW	0	Completion Timeout Value

[Table 73] PCI Express Device Status 2 Register

Bits	Type	Default Value	Description
15:0	RsvdZ	0	Reserved

[Table 74] PCI Express Link Capabilities 2 Register

Bits	Type	Default Value	Description

31:9	RsvdP	0	Reserved
8	RO	0	Cross-Link Supported (N/A)
7:1	RO	7h	Supported Link Speeds 001b: 2.5 GT/s (Gen 1) 010b: 5.0 GT/s (Gen 2) 100b: 8 GT/s (Gen 3)
0	RsvdP	0	Reserved

[Table 75] PCI Express Link Control 2 Register

Bits	Type	Default Value	Description
15:12	RWS/RsvdP	0	Compliance De-emphasis
11	RWS/RsvdP	0	Compliance SOS
10	RWS/RsvdP	0	Enter Modified Compliance
9:7	RWS/RsvdP	0	Transmit Margin
6	HwInit	0	Select De-Emphasis
5	RWS/RsvdP	0	Hardware Autonomous Speed Disable
4	RWS/RsvdP	0	Enter Compliance
3:0	RWS/RsvdP	3h	Target Link Speed 1h: 2.5 GT/s (Gen 1) 2h: 5.0 GT/s (Gen 2) 3h: 8 GT/s (Gen 3)

[Table 76] PCI Express Link Status 2 Register

Bits	Type	Default Value	Description
15:6	RsvdP	0	Reserved
5	RW1CS	0	Link Equalization Request
4	ROS	0	Equalization Phase 3 Successful
3	ROS	0	Equalization Phase 2 Successful
2	ROS	0	Equalization Phase 1 Successful
1	ROS	0	Equalization Complete
0	RO	1	Current De-Emphasis

5.1.7 Advanced Error Reporting Registers

[Table 77] Advanced Error Reporting Capability Register Summary

Start Address	End Address	Symbol	Description
100h	103h	AERID	AER Capability ID
104h	107h	AERUCES	AER Uncorrectable Error Status
108h	10Bh	AERUCEM	AER Uncorrectable Error Mask
10Ch	10Fh	AERUCESEV	AER Uncorrectable Error Severity
110h	113h	AERCES	AER Correctable Error Status
114h	117h	AERCEM	AER Correctable Error Mask
118h	11Bh	AERCC	AER Advanced Error Capabilities and Control
11Ch	12Bh	AERHL	AER Header Log

[Table 78] AER Capability ID Register

Bits	Type	Default Value	Description

31:20	RO	148h	Next Pointer (Points to Secondary PCI Express Extended Capability Header Offset)
19:16	RO	2h	Capability Version
15:0	RO	1h	Capability ID

[Table 79] AER Uncorrectable Error Status Register

Bits	Type	Default Value	Description
31:27	RsvdZ	0	Reserved
26	RW1CS	0	Poisoned TLP Egress Blocked Status (N/A)
25	RW1CS	0	TLP Prefix Blocked Error Status (N/A)
24	RW1CS	0	Atomic Op Egress Blocked Status (N/A)
23	RW1CS	0	MC Blocked TLP Status (N/A)
22	RW1CS	0	Uncorrectable Internal Error Status (N/A)
21	RW1CS	0	ACS Violation Status (N/A)
20	RW1CS	0	Unsupported Request Error Status
19	RW1CS	0	ECRC Error Status
18	RW1CS	0	Malformed TLP Status
17	RW1CS	0	Receiver Overflow Status
16	RW1CS	0	Unexpected Completion Status
15	RW1CS	0	Completer Abort Status
14	RW1CS	0	Completion Timeout Status
13	RW1CS	0	Flow Control Protocol Error Status
12	RW1CS	0	Poisoned TLP Status
11:6	RsvdZ	0	Reserved
5	RW1CS	0	Surprise Down Error Status (N/A)
4	RW1CS	0	Data Link Protocol Error Status
3:1	RsvdZ	0	Reserved
0	Undefined	0	Undefined

[Table 80] AER Uncorrectable Error Mask Register

Bits	Type	Default Value	Description
31:27	RsvdZ	0	Reserved

26	RWS	0	Poisoned TLP Egress Blocked Mask (N/A)
25	RWS	0	TLP Prefix Blocked Error Mask (N/A)
24	RWS	0	Atomic Op Egress Blocked Mask (N/A)
23	RWS	0	MC Blocked TLP Mask (N/A)
22	RWS	1	Uncorrectable Internal Error Mask (N/A)
21	RWS	0	ACS Violation Mask (N/A)
20	RWS	0	Unsupported Request Error Mask
19	RWS	0	ECRC Error Mask
18	RWS	0	Malformed TLP Mask
17	RWS	0	Receiver Overflow Mask
16	RWS	0	Unexpected Completion Mask
15	RWS	0	Completer Abort Mask
14	RWS	0	Completion Timeout Mask
13	RWS	0	Flow Control Protocol Error Mask
12	RWS	0	Poisoned TLP Mask
11:6	RsvdZ	0	Reserved
5	RWS	0	Surprise Down Error Mask (N/A)
4	RWS	0	Data Link Protocol Error Mask
3:1	RsvdZ	0	Reserved
0	Undefined	0	Undefined

[Table 81] AER Uncorrectable Error Severity Register

Bits	Type	Default Value	Description
31:27	RsvdP	0	Reserved
26	RWS	0	Poisoned TLP Egress Blocked Severity (N/A)
25	RWS	0	TLP Prefix Blocked Error Severity (N/A)
24	RWS	0	Atomic Op Egress Blocked Severity (N/A)
23	RWS	0	MC Blocked TLP Severity (N/A)
22	RWS	1	Uncorrectable Internal Error Severity (N/A)
21	RWS	0	ACS Violation Severity (N/A)
20	RWS	0	Unsupported Request Error Severity
19	RWS	0	ECRC Error Severity
18	RWS	1	Malformed TLP Severity
17	RWS	1	Receiver Overflow Severity
16	RWS	0	Unexpected Completion Severity
15	RWS	0	Completer Abort Severity
14	RWS	0	Completion Timeout Severity
13	RWS	1	Flow Control Protocol Error Severity
12	RWS	0	Poisoned TLP Severity
11:6	RsvdP	0	Reserved
5	RWS	1	Surprise Down Error Severity (N/A)
4	RWS	1	Data Link Protocol Error Severity
3:1	RsvdP	0	Reserved
0	Undefined	0	Undefined

[Table 82] AER Correctable Error Status Register

Bits	Type	Default Value	Description
31:16	RsvdZ	0	Reserved

15	RW1CS	0	Header Log Overflow Status (N/A)
14	RW1CS	0	Corrected Internal Error Status (N/A)
13	RW1CS	0	Advisory Non-Fatal Error Status
12	RW1CS	0	Replay Timer Timeout Status
11:9	RsvdZ	0	Reserved
8	RW1CS	0	Replay Number Rollover Status
7	RW1CS	0	Bad DLLP Status
6	RW1CS	0	Bad TLP Status
5:1	RsvdZ	0	Reserved
0	RW1CS	0	Received Error Status

[Table 83] AER Correctable Error Mask Register

Bits	Type	Default Value	Description
31:16	RsvdP	0	Reserved
15	RWS	0	Header Log Overflow Status (N/A)
14	RWS	1	Corrected Internal Error Mask (N/A)
13	RWS	1	Advisory Non-Fatal Error Mask
12	RWS	0	Replay Timer Timeout Mask
11:9	RsvdP	0	Reserved
8	RWS	0	Replay Number Rollover Mask
7	RWS	0	Bad DLLP Mask
6	RWS	0	Bad TLP Mask
5:1	RsvdP	0	Reserved
0	RWS	0	Received Error Mask

[Table 84] AER Capabilities and Control Register

Bits	Type	Default Value	Description
31:13	RsvdP	0	Reserved
12	RO	0	Completion Timeout Prefix/Header Log Capable (N/A)
11	ROS	0	TLP Prefix Log Present (N/A)
10	RWS	0	Multiple Header Recording Enable (N/A)
9	RO	0	Multiple Header Recording Capable (N/A)
8	RWS	0	ECRC Check Enable
7	RO	1	ECRC Check Capable
6	RWS	0	ECRC Generation Enable
5	RO	1	ECRC Generation Capable
4:0	ROS	0	First Error Pointer

[Table 85] AER Header Log Register

Bits	Type	Default Value	Description
127:120	ROS	0	Header Byte 0
119:112	ROS	0	Header Byte 1

111:104	ROS	0	Header Byte 2
103:96	ROS	0	Header Byte 3
95:88	ROS	0	Header Byte 4
87:80	ROS	0	Header Byte 5
79:72	ROS	0	Header Byte 6
71:64	ROS	0	Header Byte 7
63:56	ROS	0	Header Byte 8
55:48	ROS	0	Header Byte 9
47:40	ROS	0	Header Byte 10
39:32	ROS	0	Header Byte 11
31:24	ROS	0	Header Byte 12
23:16	ROS	0	Header Byte 13
15:8	ROS	0	Header Byte 14
7:0	ROS	0	Header Byte 15

[Table 86] Secondary PCI Express Capability Register Summary

Start Address	End Address	Symbol	Description
168h	16Bh	SPXID	Secondary PCI Express Capability
16Ch	16Fh	PXLC3	PCI Express Link Control 3
170h	173h	PXLE	PCI Express Lane Error Status
174h	175h	PXL0EC	PCI Express Lane 0 Equalization Control
176h	177h	PXL1EC	PCI Express Lane 1 Equalization Control
178h	179h	PXL2EC	PCI Express Lane 2 Equalization Control
17Ah	17Bh	PXL3EC	PCI Express Lane 3 Equalization Control

[Table 87] Secondary PCI Express Capability ID Register

Bits	Type	Default Value	Description
31:20	RO	188h	Next Pointer (Samsung Vendor Specific Capability)
19:16	RO	1h	Capability Version
15:0	RO	0019h	Capability ID (Secondary PCI Express Extended capability)

[Table 88] PCI Express Link Control 3 Register

Bits	Type	Default Value	Description
31:2	Rsvdp	0	Reserved
1	Rsvdp	0	Link Equalization Request Interrupt Enable (N/A)
0	Rsvdp	0	Perform Equalization (N/A)

[Table 89] PCI Express Lane Error Status Register

Bits	Type	Default Value	Description
31:4	Rsvdp	0	Reserved
3:0	RW1CS	0	Lane Error Status Bits

[Table 90] PCI Express Lane 0 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port Transmitter Preset

7	RsvdP	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port Transmitter Preset (N/A)

[Table 91] PCI Express Lane 1 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port Transmitter Preset
7	RsvdP	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port Transmitter Preset (N/A)

[Table 92] PCI Express Lane 2 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port Transmitter Preset
7	RsvdP	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port Transmitter Preset (N/A)

[Table 93] PCI Express Lane 3 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port Transmitter Preset
7	RsvdP	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port Transmitter Preset (N/A)

5.1.8 Device Serial Number Capability Register

[Table 94] Device Serial Number Capability Register Summary

Start Address	End Address	Symbol	Description
148h	14Bh	DSNID	Device Serial Number Capability ID
14Ch	14Fh	SNRL	Serial Number Register (Lower DW)
150h	153h	SNRU	Serial Number Register (Upper DW)

[Table 95] Device Serial Number Capability Register Header

Bits	Type	Default Value	Description
31:20	RO	158h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	3h	PCI Express Extended Capability ID

[Table 96] Serial Number Register Header (Lower DW)

Bits	Type	Default Value	Description
31:0	RO	0	Serial Number register (Lower DW) (N/A)

[Table 97] Serial Number Register Header (Upper DW)

Bits	Type	Default Value	Description
31:0	RO	0	Serial Number register (Upper DW) (N/A)

5.1.9 Power Budgeting Extended Capability

[Table 98] Power Budgeting Extended Capability Register Summary

Start Address	End Address	Symbol	Description
158h	15Bh	PBXID	Power Budgeting Extended Capability ID
15Ch	15Fh	DSR	Data Select Register
160h	163h	DR	Data Register
164h	167h	PBCR	Power Budget Capability Register

[Table 99] Power Budgeting Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	168h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	4h	PCI Express Extended Capability ID

[Table 100] Data Select Register

Bits	Type	Default Value	Description
31:8	RsvdP	0	Reserved
7:0	RW	0	Data Select

[Table 101] Data Register

Bits	Type	Default Value	Description
31:21	RsvdP	0	Reserved
20:18	RO	0	Power Rail (N/A)
17:15	RO	0	Type (N/A)
14:13	RO	0	PM State (N/A)
12:10	RO	0	PM Sub State (N/A)
9:8	RO	0	Data Scale (N/A)
7:0	RO	0	Base Power

[Table 102] Power Budget Capability Register

Bits	Type	Default Value	Description
7:1	RsvdP	0	Reserved
0	HwInit	0	System Allocated (N/A)

5.1.10 Latency Tolerance Reporting Capability Registers

[Table 103] Latency Tolerance Reporting Capability Register Summary

Start Address	End Address	Symbol	Description
188h	18Bh	LTRID	Latency Tolerance Reporting(LTR) Capability ID
18Ch	18Dh	LTRMSLR	LTR Max Snoop Latency Register
18Eh	18Fh	LTRMNSLR	LTR Max No-Snoop Latency Register

[Table 104] LTR Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	190h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	18h	PCI Express Extended Capability ID

[Table 105] LTR Max Snoop latency Register

Bits	Type	Default Value	Description
15:13	RsvdP	0	Reserved
12:10	RW	0	Max Snoop latency Scale
9:0	RW	0	Max Snoop latency Value

[Table 106] LTR Max No Snoop latency Register

Bits	Type	Default Value	Description
15:13	RsvdP	0	Reserved
12:10	RW	0	Max No Snoop latency Scale
9:0	RW	0	Max No Snoop latency Value

5.1.11 L1 Substates Capability Registers

[Table 107] L1 Substate Capability Register Summary

Start Address	End Address	Symbol	Description
190h	193h	L1SCID	L1 Substate Capability ID
194h	197h	L1SCR	L1 Substate Capability Register
198h	19Bh	L1SC1R	L1 Substate Control 1 Register
19Ch	19Fh	L1SC2R	L1 Substate Control 2 Register

[Table 108] L1 Substates Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	0	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	1Eh	PCI Express Extended Capability ID

[Table 109] L1 Substates Capability Register

Bits	Type	Default Value	Description
31:24	RsvdP	0	Reserved
23:19	HwInit	5h	Port Power on value
18	RsvdP	0	Reserved
17:16	HwInit	0	Port T_Power_on scale
15:08	HwInit	46h	Port Common_mode_restore_time
4	HwInit	0	L1 PM Substates Supported
3	HwInit	0	ASPM PM L1.1 Supported
2	HwInit	0	ASPM PM L1.2 Supported
1	HwInit	0	PCI PM L1.1 Supported
0	HwInit	0	PCI PM L1.2 Supported

[Table 110] L1 Substates Control1 Register

Bits	Type	Default Value	Description
31:29	RW	0	LTR L1.2 Threshold Scale
28:26	RsvdP	0	Reserved
25:16	RW	0	LTR L1.2 Threshold value
15:8	RsvdP	0	Common_mode_restore_time
7:4	RsvdP	0	Reserved
3	RW	0	ASPM PM L1.1 Supported
2	RW	0	ASPM PM L1.2 Supported
1	RW	0	PCI PM L1.1 Supported
0	RW	0	PCI PM L1.2 Supported

[Table 111] L1 Substates Control2 Register

Bits	Type	Default Value	Description
31:8	RsvdP	0	Reserved
7:3	RW	5	T_POWER_ON Value
2	RsvdP	0	Reserved
1:0	RW	0	T_POWER_ON Scale

5.2 NVM Express Registers

5.2.1 Register Summary

[Table 112] Register Summary

Start Address	End Address	Name	Type
00h	07h	CAP	Controller Capabilities
08h	0Bh	VS	Version
0Ch	0Fh	INTMS	Interrupt Mask Set
10h	13h	INTMC	Interrupt Mask Clear
14h	17h	CC	Controller Configuration
18h	1Bh	Reserved	Reserved
1Ch	1Fh	CSTS	Controller Status
20h	23h	Reserved	Reserved
24h	27h	AQA	Admin Queue Attributes
28h	2Fh	ASQ	Admin Submission Queue Base Address
30h	37h	ACQ	Admin Completion Queue Base Address
38h	EFFh	Reserved	Reserved
F00h	FFFh	Reserved	Command Set Specific
1000h	1003h	SQ0TDBL	Submission Queue 0 Tail Doorbell (Admin)
1000h + (1 * (4 << CAP.DSTRD))	1003h + (1 * (4 << CAP.DSTRD))	CQ0HDBL	Completion Queue 0 Head Doorbell (Admin)
...			
1000h+ (2y * (4 << CAP.DSTRD))	1003h + (2y * (4 << CAP.DSTRD))	SQyTDVL	Submission Queue y Tail Doorbell
1000h + ((2y + 1) * (4 << CAP.DSTRD))	1003h + ((2y + 1) * (4 << CAP.DSTRD))	CQYHDBL	Completion Queue y Head Doorbell

5.2.2 Controller Registers

[Table 113] Controller Capabilities

Bits	Type	Name	Default Value	Description
63:56	RO		0h	Reserved
55:52	RO	MPSMAX	Fh	Memory Page Size Maximum (Maximum is 128MB)
51:48	RO	MPSMIN	0	Memory Page Size Minimum (Minimum is 4KB)
47:45	RO		0	Reserved
44:37	RO	CSS	1h	Command Sets Supported 1h: NVM command set
36	RO		0	Reserved
35:32	RO	DSTRD	0	Doorbell Stride 0: Stride of 4 bytes
31:24	RO	TO	28h	Timeout 28h: 20 seconds
23:19	RO		0	Reserved
18:17	RO	AMS	1	Arbitration Mechanism Supported Weighted Round Robin Supported
16	RO	CQR	1	Contiguous Queues Required
15:00	RO	MQES	3FFFh	Maximum Queue Entries Supported (16384 entries supported)

[Table 114] Version

Bits	Type	Name	Default Value	Description
31:16	RO	MJR	1h	Major Version Number
15:08	RO	MNR	2h	Minor Version Number
07:00	RO	Reserved	00h	Reserved

NOTE:
The SM963 supports NVM Express version 1.2 (partially).

[Table 115] Interrupt Mask Set

Bits	Type	Name	Default Value	Description
31:00	RW1S	IVMS	0	Interrupt Vector Mask Set

[Table 116] Interrupt Mask Clear

Bits	Type	Name	Default Value	Description
31:00	RW1C	IVMC	0	Interrupt Vector Mask Clear

[Table 117] Controller Configuration

Bits	Type	Name	Default Value	Description
31:24	RO	-	0	Reserved
23:20	RW	IOCQES	0	I/O Completion Queue Entry Size (Configured as a power of 2) (Should be set to 4 for a 16 byte entry size)
19:16	RW	IOSQES	0	I/O Submission Queue Entry Size (Configured as a power of 2) (Should be set to 6 for a 64 byte entry size)
15:14	RW	SHN	0	Shutdown Notification 0h: No notification 1h: Normal shutdown notification 2h: Abrupt shutdown notification 3h: Reserved CSTS.SHST indicates shutdown status.
13:11	RW	AMS	0	Arbitration Mechanism Selected 0h: Round Robin No other values supported.
10:7	RW	MPS	0	Memory Page Size MPS is 2^(12+MPS) Shall be within CAP.MPSMAX and CAP.MPSMIN ranges.
6:4	RW	CSS	0	Command Set Selected 0h: NVM Command Set No other values supported
3:1	RO	-	0	Reserved
0	RW	EN	0	Enable When set to 1, controller shall process commands. When cleared to 0, controller shall not process commands. This field is subject to CSTS.RDY and CAP.TO restrictions.

[Table 118] Controller Status

Bits	Type	Name	Default Value	Description
31:4	RO	-	0	Reserved
3:2	RO	SHST	0	Shutdown Status 0h: Normal operation, no shutdown requested 1h: Shutdown processing occurring 2h: Shutdown processing complete 3h: Reserved
1	RO	CFS	0	Controller Fatal Status
0	RO	RDY	0	1h: Controller ready to process commands 0h: Controller shall not process commands.

[Table 119] Admin Queue Attributes

Bits	Type	Name	Default Value	Description
31:28	RO	-	0	Reserved
27:16	RW	ACQS	0	Admin Completion Queue Size Max: 4096 (Value of 4095h - 0's based value)
15:12	RO	-	0	Reserved
11:0	RW	ASQS	0	Admin Submission Queue Size Max: 4096 (Value of 4095h - 0's based value)

[Table 120] Admin Submission Queue Base Address

Bits	Type	Name	Default Value	Description
63:12	RW	ASQB	0	Admin Submission Queue Base Address
11:0	RO	-	0	Reserved

[Table 121] Admin Completion Queue Base Address

Bits	Type	Name	Default Value	Description
63:12	RW	ACQB	0	Admin Completion Queue Base Address
11:0	RO	-	0	Reserved

[Table 122] Submission Queue Tail y Doorbell

Bits	Type	Name	Default Value	Description
31:16	RO		0	Reserved
15:0	RW	SQT	0	Submission Queue Tail

[Table 123] Completion Queue Head y Doorbell

Bits	Type	Name	Default Value	Description
31:16	RO		0	Reserved
15:0	RW	CQH	0	Completion Queue Head

6.0 Supported Command Set

The Admin command sets and NVM I/O command sets of Samsung SSD SM963 are defined in compliant with NVM Express specification revision 1.2.

6.1 Admin Command Set

The Admin command set is the commands that are submitted to the Admin Submission Queues. The detailed specifications are described in NVM Express specification document.

[Table 124] Opcode for Admin Commands

Opcode (Hex)	Command Name
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Feature
0Ah	Get Feature
0Ch	Asynchronous Event Request
0Dh	Namespace Management
10h	Firmware Activate
11h	Firmware Image Download
15h	Namespace Attachment
80h – BFh	I/O Command Set Specific
C0h – FFh	Vendor Specific

6.1.1 Identify Command

The Identify Command returns the data described below.

[Table 125] Identify Controller Data Structure

Bytes	O/M	Default Value	Description
1:0	M	144Dh	PCI Vendor ID
3:2	M	144Dh	PCI Subsystem Vendor ID
23:4	M	S###N##########	Serial Number (ASCII), #:Variables
63:24	M	480GB : SAMSUNG MZ1KW480HMHQ-00003 960GB : SAMSUNG MZ1KW960HMJP-00003 1.92TB : SAMSUNG MZ1KW1T9HMLS-00003	Model Number (ASCII)
71:64	M	CXU#####	Firmware Revision, #:Variables
72	M	2h	Recommended Arbitration Burst
75:73	M	002538h	IEEE OUI
76	O	0	Multi-Interface Capabilties and Namespace Sharing Capability Bit 2: 1h - Controller is associated with an SR-IOV Virtual Function 0h - Controller is associated with a PCI Function. Bit 1: 1h - Device has Two or More controller 0h - Device has One Controller Bit 0: 1h - Device has Two or More physical PCI Express ports 0h - Device has One PCI Express port
77	M	6h	Maximum Data Transfer Size 6h: 256KB
79:78	M	02h	Controller ID (CNTLID)

83:80	M	0x10200	Controller Version
87:84	M	0x7a1200	RTD3 Resume Latency
91:88	M	0x7a1200	RTD3 Entry Latency
95:92	M	0h	OAES_Reserved
239:96	-	0h	Reserved
255:240	M	-	NVMe Management Interface Specification for Definition
257:256	M	0Eh	Optional Admin Command Support Bits 15:4 - Reserved Bit 3: 1h - Namespace Management and Namespace Attachment Commands Supported (SM963 conditionally supports the Namespace Management and Namespace Attachment command(NVMe v1.2 specification) for reconfigurable overprovisioning) Bit 2: 1h – Firmware Activate/Download Supported Bit 1: 1h Format NVM Supported Bit 0: 0 Security Send and Security Receive Not Supported
258	M	7h	Abort Command Limit (Maximum number of concurrently outstanding Abort commands) (0's based value)
259	M	3h	Asynchronous Event Request Limit (Maximum number of concurrently outstanding Asynchronous Event Request commands) (0's based value)
260	M	17h	Firmware Updates Bits 7:4 – Reserved Bits 3:1 – Number of firmware slots Bit 0 – 1h Slot 1 is read only
261	M	3h	Log Page Attributes Bits 7:2 – Reserved Bit 1: 1h Command Effects log page Bit 0: 0h SMART data is global for all namespaces
262	M	3Fh	Error Log Page Entries (Number of Error Information log entries stored by controller) (0's based value)
263	M	0h	Number of Power States Support (0's based value)
264	M	1h	Admin Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates Admin Vendor Specific Commands use the format defined in NVM Express 1.0c Figure 8.
265	O	0h	Autonomous Power State Transition Attributes (APSTA)
267:266	M	53h	Warning Composite Temperature Threshold
269:268	M	54h	Critical Composite Temperature Threshold
271:270	O	0h	Maximum Time for Firmware Activation
275:272	O	0h	Host Memory Buffer Preferred Size
279:276	O	0h	Host Memory Buffer Minimum Size
295:280	O	37E436B0h * 512 (480GB) 6FC81AB0h * 512 (960GB) DF8FE2B0h * 512 (1920GB)	Total NVM Capacity
311:296	O	0h	Unallocated NVM Capacity
315:312	O	0h	RPMBS
511:316	-	-	Reserved

512	M	66h	Submission Queue Entry Size Bits 7:4 – 6h Max SQES (64 bytes) Bits 3:0 – 6h Required SQES (64 bytes)
513	M	44h	Completion Queue Entry Size Bits 7:4 – 4h Max SQES (16 bytes) Bits 3:0 – 4h Required SQES (16 bytes)
515:514		0h	Reserved
519:516	M	1h	Number of Namespaces
521:520	M	1Fh	Optional NVM Command Support Bits 15:6 – Reserved Bit 5 – 1h Reservations Supported 0h Not support Reservations Bit 4 – 1h Save field in Set Feature & Select field in Get Feature Supported 0h Not support Save field in Set Feature & Select field in Get Feature Bit 3 – 1h Write Zeros Supported 0h Not support Write Zeros Bit 2 – 1h Dataset Management Supported 0h Not support Dataset Management Bit 1 – 1h Write Uncorrectable Supported 0h Not support Write Uncorrectable Bit 0 – 1h Compare Supported 0h Not support Compare
523:522	M	0h	Fused Operation Support Bits 15:1 – Reserved Bit 0 – 0h Compare/Write Fused Operation Not Supported
524	M	0h	Format NVM Attributes Bits 7:3 – Reserved Bit 2 – 1h Cryptographic Erase Bit 1 – 1h Secure Erase Per Namespace Bit 0 – 0h Format Per Namespace
525	M	0h	Volatile Write Cache 0h – No VWC present
527:526	M	3Fh	Atomic Write Unit Normal
529:528	M	0h	Atomic Write Unit Power Fail (0's based value)
530	M	1h	NVM Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates NVM Vendor Specific Commands use the format defined in NVM Express specification
531	M	0h	Reserved
533:532	O	0h	ACWU
534:533	M	0h	Reserved
539:536	O	0h	No SGL support
703:540	-	0h	Reserved
I/O Command Set Attributes			
2047:704	-	0h	Reserved
Power State Descriptors			
2079:2048	M	refer to '[Table 126] Identify Power State Descriptor Data Structure'	Power State 0 Descriptor
2111:2080	O	0h	N/A
2143:2112	O	0h	N/A
...	-	0h	N/A
3071:3040	O	0h	Power State 31 Descriptor (N/A)
Vendor Specific			

4095:3072	-	-	Samsung Reserved

[Table 126] Identify Power State Descriptor Data Structure

Bits	Power State 0	Description
255:184	0h	Reserved
183:182	0h	Active Power Scale(APS)
181:179	0h	Reserved
178:176	0h	Active Power Workload(APW)
175:160	0h	Active Power(ACTP)
159:152	0h	Reserved
151:150	0h	Idle Power Scale(IPS)
149:144	0h	Reserverd
143:128	0h	Idle Power(IDLP)
127:125	0h	Reserved
124:120	0h	Relative Write Latency
119:117	0h	Reserved
116:112	0h	RelativeWriteThroughput
111:109	0h	Reserved
108:104	0h	RelativeReadLatency
103:101	0h	Reserved
100:96	0h	RelativeReadThroughput
95:64	5h	Exit Latency
63:32:00	5h	EntryLatency (100us)
31:26:00	0h	Reserved
25	0h	Non-Operational State
24	0h	Max Power Scale
23:16	0h	Namespace Utilization A device may report Namespace Utilization equal to Namespace Capacity at all times if the product is not targeted for thin provisioning environments
15:00	384h	Maximum Power

[Table 127] Identify Namespace Data Structure

Bytes	O/M	Default Value		Description
7:0	M	480GB 960GB 1920GB	37E436B0h (512B) 6FC81AB0h (512B) DF8FE2B0h (512B)	Namespace Size
15:8	M	480GB 960GB 1920GB	37E436B0h (512B) 6FC81AB0h (512B) DF8FE2B0h (512B)	Namespace Capacity
23:16	M	-		Namespace Utilization A device may report Namespace Utilization equal to Namespace Capacity at all times if the product is not targeted for thin provisioning environments
24	M	2h		Namespace Features Bits 7:3 Reserved Bit 2 : Deallocated or Unwritten Logical Block error Bit 1 : NAWUN, NAWUPF, NACWU Bit 0: Thin provisioning not supported
25	M	1h		Number of LBA Formats
26	M	0h		Formatted LBA Size Bits 7:5 – Reserved Bit 4: Metadata interleaved or separate (based on LBA format) Bit 3:0 – Indicates LBA format
27	M	0h		Metadata Capabilities Bits 7:2 – Reserved Bit 1 – Supports Metadata as separate buffer Bit 0 – Supports Metadata as extended LBA
28	M	0h		End-to-end Data Protection Capabilities Bits 7:5 – Reserved Bit 4 – Supports protection information as last 8 bytes of Metadata Bit 3 – Supports protection information as first 8 bytes of metadata Bit 2 – Supports Type 3 protection information Bit 1 – Supports Type 2 protection information Bit 0 – Supports Type 1 protection information
29	M	0h		End-to-End Data Protection Type Settings Bits 7:4 – Reserved Bit 3 – 1: Protection information transferred as first 8 bytes of metadata Bit 3 – 0: Protection information transferred as last 8 bytes of metadata Bit 2:0 – 000b: Protection information disabled Bit 2:0 – 1h: Protection type 1 enabled Bit 2:0 – 2h: Protection type 2 enabled Bit 2:0 – 3h: Protection type 3 enabled
30	O	0h		Namespace Multi-path I/O and Namespace sharing Capabilities (NMIC) Bits 7:1 - Reserved Bit 0 - 1 : Accessible by two or more controllers Bit 0 - 0 : Private namespace

31	O	0h	Reservation Capabilities (RESCAP) Bits 7 - Reserved Bits 6 - 1: Namespace supports the Exclusive Access (All Registrants reservation type) Bit 5 - 1 : Namespace supports the Write Exclusive (All Registrants reservation type) Bit 4 - 1 : Namespace supports the Exclusive Access (Registrants only reservation type) Bit 3 - 1 : Namespace supports the Write Exclusive (Registrants only reservation type) Bit 2 - 1 : Namespace supports the Exclusive Access Reservation type Bit 1 - 1 : Namespace supports the Write Exclusive Reservation type Bit 0 - 1 : Namespace supports the Persist Through Power Loss capability
32	O	80h	Format Progress Indicator(FPI) Bit 7 - 1 : Format Progress Indicator support Bit 6:0 - remained percentage
33	-	Reserved	
35:34	O	1FFh (512B) / 3Fh (4KB)	Namespace Atomic Write Unit Normal
37:36	O	7h (512B) / 0h (4KB)	Namespace Atomic Write Unit Power Fail
39:38	O	0h	Namespace Atomic Compare & Write Unit
41:40	O	1FFh (512B) / 3Fh (4KB)	Namespace Atomic Boundary Size Normal
43:42	O	0h	Namespace Atomic Boundary Offset
45:44	O	7h (512B) / 0h (4KB)	Namespace Atomic Boundary Size Power Fail
47:46	-	Reserved	
63:48	O	37E436B0h * 512 (480GB) 6FC81AB0h * 512 (960GB) DF8FE2B0h * 512 (1920GB)	NVM Capacity (NVMCAP)
103:64	-	0h	Reserved
119:104	O	################002538##########h	Namespace Globally Unique Identifier (NGUID) #:Variables *NGUID specifies data in a big endian format.
127:120	O	0h	IEEE Extended Unique Identifier(EUI64) #:Variables *EUI64 specifies data in a big endian format.
131:128	M	refer to '[Table 128] LBA Format 0 Data Structure'	LBA Format 0 Support
135:132	O	refer to '[Table 129] LBA Format 1 Data Structure'	LBA Format 1 Support
139:136	O	0h	LBA Format 2 Support
143:140	O	0h	LBA Format 3 Support
147:144	O	0h	LBA Format 4 Support (N/A)
…			
191:188	O	0h	LBA Format 15 Support (N/A)
383:192	-	0h	Reserved
Vendor Specific			
4095:384	-	-	Samsung Reserved

[Table 128] LBA Format 0 Data Structure

Bits	Name	Default Value	Description
31:26		0	Reserved
25:24	RP	0	Relative Performance
23:16	LBADS	9h	LBA Data Size
15:00	MS	0	Metadata Size

[Table 129] LBA Format 1 Data Structure

Bits	Name	Default Value	Description
31:26		0	Reserved
25:24	RP	0	Relative Performance
23:16	LBADS	Ch	LBA Data Size
15:00	MS	0	Meta data Size

6.2 NVM Express I/O Command Set

[Table 130] Opcode for NVM Express I/O Commands

Opcode (Hex)	Command Name
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
05h	Compare
08h	Write Zeroes
09h	Dataset Management

NOTE:
1) Deallocate feature in Dataset Management command is only supported in the Samsung SSD SM963.

6.3 SMART/Health Information

[Table 131] SMART/Health Information Log

Bytes	Default Value	Attribute Description
0	0	Critical Warning Bit 7:5 – Reserved Bit 4 – 1h: the volatile memory backup device has failed. (only valid if the controller has a volatile memory backup solution) Bit 3 – 1h: the media has been placed in read only mode Bit 2 – 1h: the device reliability has been degraded due to significant media related errors or any internal error that degrades device reliability Bit 1 – 1h: the temperature has exceeded a critical threshold Bit 0 – 1h: the available spare space has fallen below the threshold
2:1	current temp.	Temperature
3	100	Available Spare
4	10	Available Spare Threshold
5	0	Percentage Used
31:6	-	Reserved
47:32	0	Data Units Read
63:48	0	Data Units Written
79:64	0	Host Read Commands
95:80	0	Host Write Commands
111:96	0	Controller Busy Time
127:112	0	Power Cycles
143:128	0	Power On Hours
159:144	0	Unsafe Shutdowns
175:160	0	Media Errors
191:176	0	Number of Error Information Log Entries
511:192	-	Reserved
195:192	0	Warning Composite Temperature Time
199:196	0	Critical Composite Temperature Time
201:200	0	Temperature Sensor 1
203:202	0	Temperature Sensor 2
205:204	0	Temperature Sensor 3
207:206	0	Temperature Sensor 4
209:208	0	Temperature Sensor 5
211:210	0	Temperature Sensor 6
213:212	0	Temperature Sensor 7
215:213	0	Temperature Sensor 8
511:216	-	Reserved

7.0 SPOR Specification (Sudden Power Off and Recovery)

7.1 Data Recovery in Sudden Power off

If power interruption is detected, SSD dumps all cached user data and meta data to NAND Flash. SSD could protect even the user data in DRAM from sudden power off while SSD is used with cache on. Commonly, data is protected all of the operation period.

7.2 Time to Ready Sequence

In normal power-off recovery status, SSD needs less than 8 seconds to reach operating mode where SSD works perfectly with cache-on state. SSD is ready to respond identify Device command during FTL OPEN. When the sudden power-off occurs, the user data in DRAM will be dumped into the NAND Flash using the stored power in the capacitor. In sudden power-off recovery condition, mapping data will be loaded or the FTL meta data be rebuilt perfectly for initial max. 10 seconds. During this period, Identify Device command is still supported. It is called SPOR.
(Sudden Power Off and Recovery)

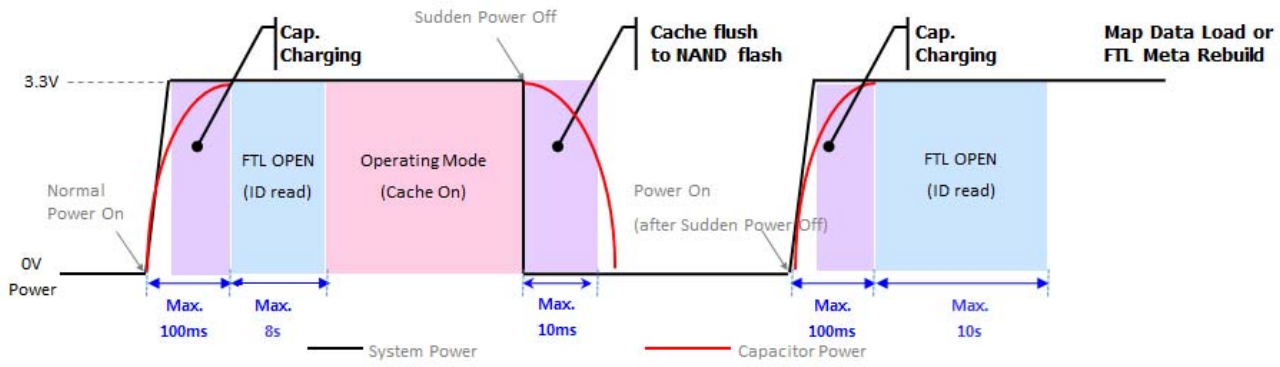


Figure 3. Sudden Power on-off operation

[Table 132] Device Ready Time for Normal Read / Write Operation after Sudden Power Off

	480GB	960GB	1.92TB
Max. Open Time (sec)	10 s		

8.0 PRODUCT COMPLIANCE

8.1 Product regulatory compliance and Certifications

[Table 133] Certifications and Declarations

Category	Certifications
Safety	c-UL-us
	CE
	TUV
	CB
EMC	CE (EU)
	BSMI (Taiwan)
	KCC (South Korea)
	VCCI (Japan)
	RCM (Australia)
	FCC (USA)
	IC (CANADA)

The three existing compliance marks (C-Tick, A-Tick and RCM) are consolidated into a single compliance mark - the RCM.

Caution: Any changes or modifications in construction of this device which are not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE:
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications, However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio / TV technician for help.

Modifications not expressly approved by the manufacturer could void the user's authority to operated the equipment under FCC rules.

Industry Canada ICES-003 Compliance Label:

CAN ICES-3 (B)/NMB-3(B)

9.0 References

[Table 134] Standards References

Item	Website
PCI Express Base Specification Revision 3.0	http://www.pcisig.com/specifications/pciexpress/base3/
PCI Express CEM Specification Revision 3.0	http://www.pcisig.com/specifications/
NVM Express Specification Rev. 1.2	http://www.nvmexpress.org/
PCIe M.2 Electromechanical Specification Revision 1.1	http://www.pcisig.com/
Solid-State Drive Requirements and Endurance Test Method (JESD218A)	http://www.jedec.org/standards-documents/docs/jesd218a
Solid-State Drive Requirements and Endurance Test Method (JESD219A)	http://www.jedec.org/standards-documents/docs/jesd219a